Evolution from Operational Amplifier to Data Amplifier

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This article explains the difference between an operational amplifier and a wideband DC differential amplifier of the type generally referred to as a data amplifier. Several basic op-amp circuits are analyzed here, and their characteristics summarized in a comprehensive table. Also, the key parameters of a data measuring application are discussed, with the problems developed from first principles. Finally, the article reviews data acquisition applications in terms of op-amp circuits, and concludes that no presently available op amp can meet all the requirements for extracting millivolt signals from a data circuit's high level of common mode noise.

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DATA AMPLIFIERS

Wide Band DC Differential Amplifiers

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INTRODUCTION

In order to explain the difference between operational amplifiers and data measuring amplifiers (termed "Wideband DC Differential Amplifiers"), and then further, to highlight the salient features of an advanced data amplifier, a first step is to review the basic operational amplifier circuits and develop an inventory of their advantages and disadvantages. Later on, as we analyze a hypothetical data measuring application (measuring the temperature of a rocket exhaust), several important criteria for a data amplifier performance will emerge. The op amp circuits can then be compared against these criteria to see whether circuits based on off-the-shelf op amps can handle high accuracy data measurements.

Generally speaking, they can't! We can anticipate the conclusions of this article by stating that none of today's off-the-shelf op amps can simultaneously meet the DC stability, input impedance, gain-bandwidth and common mode specifications required for measuring millivolt signals in the presence of large doses of common mode noise typically encountered in data measuring situations.

For a start, therefore, we will examine the three basic op amp circuits: inverting, noninverting and differential, and justify the remarks presented in Table 1 on page 2. We also hope that the reader will benefit from the ensuing discussion, analysis and comparison of many different circuits, even if he's not particularly concerned with advanced data aquisition problems.

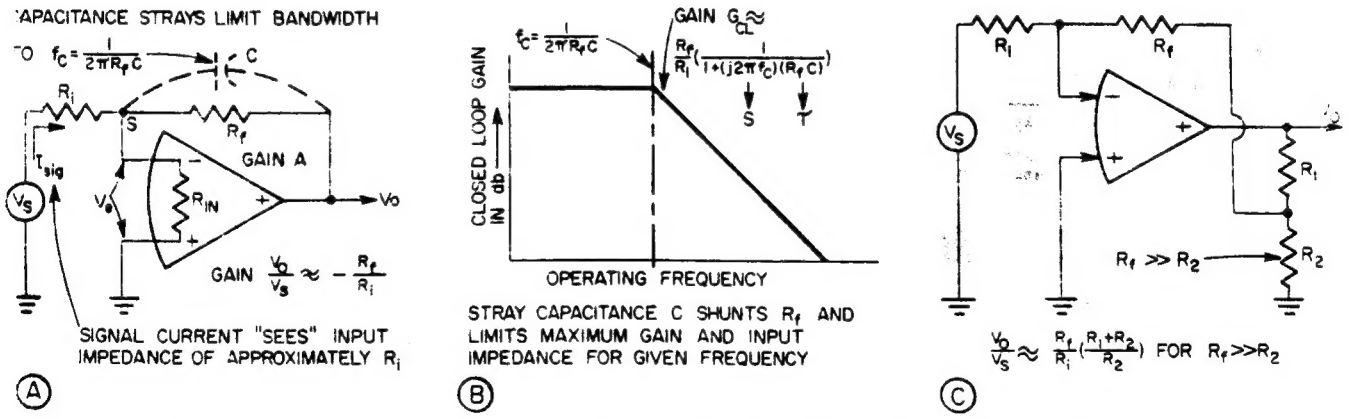


Fig. 1 - Inverting circuit is susceptible to bandwidth, gain, and input impedance limitations due to capacitance strays shunting feedback resistor (A). Closed loop gain curve (B) shows how gain rolls off at 6 db/octave when operating frequency makes reactance of C smaller than R_f. Circuit (C) is a method for achieving high gain with low resistance values, but at expense of increased noise and drift.

INVERTING CIRCUIT

We'll first review the inverting configuration because it is perhaps the best known and probably the most versitile. The basic circuit is shown in Fig. 1, and its

TABLE 1

PARAMETER	INVERTING FIG. 1A	NONINVERTING FIG. 2	DIFFERENTIAL FIG. 5	DIFFERENTIAL FIG. 8A	DIFFERENTIAL FIG. 8B (3)	DIFFERENTIAL FIG. 10
SIGNAL GAIN G_{cl}	$\frac{R_f}{R_1}$	$1 + \frac{R_1}{R_2}$	$\frac{R_2}{R_1}$	$1 + N$	$-\frac{R_3}{R_2}$	$\frac{R_5}{R_4}\left[1 + \frac{2R_1}{R_2}\right]$
DIFFERENTIAL INPUT RESISTANCE	N.A.	N.A.	$2R_1$	$R(1 + A)$	$R_1 + R_2$	$1 + \frac{R_2 A}{2R_1 + R_2}$
COMMON MODE INPUT RESISTANCE	R_1	$R_{IN}(1 + A)$ paralleled by R_{cm}	$\frac{1}{2}\left[R_1 + \frac{R_2 R_{cm}}{R_2 + R_{cm}}\right]$	$\frac{R_{cm}}{2}$	$\frac{R_1 R_2}{R_1 + R_2}$	$\frac{R_{cm}}{2}$
VOLTAGE DRIFT REFERRED TO INPUT (1)	$e_{os}\left[1 + \frac{R_1}{R_f}\right]$	e_{os}	$e_{os}\left[1 + \frac{R_1}{R_2}\right]$	$2\,e_{os}$	$4e_{os}\left[1 + \frac{R_2}{4R_3}\right]$	$e_{os}\left[2 + \frac{1 + \text{GAIN B}}{\text{GAIN A}}\right]$
CURRENT DRIFT REFERRED TO INPUT AS VOLTAGE VARIATION (2)	$i_b R_1$	$i_b R_{source}$	$i_d R_1$	$i_b R_s$	$i_b (R_1 + R_2)$	$i_b R_s + \frac{i_d R_4}{\text{GAIN A}}$
CMRR DUE TO RESISTANCE DEVIATION, K	N.A.	N.A.	$\frac{1 + G_{cl}}{4K}$	$\frac{G_{cl}}{4K}$	$\frac{1}{4K}$	$\frac{\text{GAIN A (1 + GAIN B)}}{4\,K}$
CMRR DUE TO AMPLIFIER GAIN INEQUALITY	N.A.	$\frac{A}{(A_2 - A_1)}$ Listed In Data Sheet	$\frac{A}{(A_2 - A_1)}$ Listed In Data Sheet	$\frac{A}{2(A_2 - A_1)}$	N.A.	FIRST STAGE $\frac{A}{2(A_2 - A_1)}$ paralleled by SECOND STAGE $\frac{(\text{GAIN A})\,A}{(A_2 - A_1)}$
OVERALL ERROR e_{cm} / V_{cm} CMRR = $\frac{1}{e_{cm}/V_{cm}}$	N.A.	$\frac{A_2 - A_1}{A}$	$\frac{4\,K}{1 + G_{cl}} + \frac{A_2 - A_1}{A}$	$\frac{4\,K}{G_{cl}} + \frac{2(A_2 - A_1)}{A}$	$4\,K$	$\frac{2(A_2 - A_1)}{A} + \frac{(A_2 - A_1)}{(\text{GAIN A})A} + \frac{4K}{\text{GAIN A}(1 + \text{GAIN B})}$

NOTES:

1. e_{os} is amplifier offset voltage drift due to temperature, i.e., $\left(\frac{\Delta e}{\Delta T}\right)\Delta T$
2. i_b is the temperature-induced bias current drift, while i_d is difference-current drift
3. Calculations shown for $R_1 = R_3$
4. Amplifier's parameters assumed equal in magnitude, not necessarily in sign, for circuits 8A, 8B, and 10.

closed loop gain, V_o/V_s, is very nearly the ratio of feedback to input resistor R_f/R_i. If the op amp's internal, or open loop gain is high (10,000 volts/volt and upwards), then the error voltage V_e at the summing junction, S, will be very small: less than 1 mV for a gain of 10,000 and often a matter of microvolts, for a full scale $\pm$10 volts output. In effect, therefore, point S remains within a whisker of ground potential (called a virtual ground), so that the input signal current I_{sig} is very nearly V_s/R_i. More accurately, I_{sig} would be $(V_s - V_e)/R_i$, but V_e is just a few microvolts, and will generally be negligible for our purposes of determining input impedance.

Because the summing junction is to all intents and purposes at ground potential, the inverting circuit's input impedance, so far as the signal source is concerned, is simply equal to the value of the input resistance R_i. Now this brings us to the major limitations associated with inverting amplifiers.

The inevitable stray capacitance (rarely less than 1 pf) in parallel with the feedback resistance R_f is the cause of the difficulty. The stray capacitance C shunts R_f and limits the circuit's frequency response to a frequency that makes the leakage reactance $1/2\pi f_c C$ equal to R_f. That is, bandwidth is restricted to $f_c=1/2\pi R_f C$ (Figure 1B). This limitation does not concern frequency alone, but gets into the act when high gain and high input impedance are simultaneously required.

We can easily see why. First of all, high input impedance requires a high value for R_i. But if the amplifier must operate at high closed loop gain, then the feedback resistance R_f must be higher than the input resistance in the ratio R_f= Gain x R_i. For example, if the input impedance must be 1 megohm to avoid source loading effects, and a 60dB (1000:1) closed loop gain is required, the feedback resistance will become 1000 x 1 megohm = 1000 megohms. The frequency at which the reactance of 1 pf leakage capacitance equals 1000 megohms is only about 160Hz, which makes a pretty spectacular bandwidth limitation. Actually, 1000-megohm high stability resistors don't exist, so a different circuit, such as Figure 1C, would be required for this level of gain.

Generally speaking, the inverting circuit is the wrong approach to adopt for high input impedance, and the noninverting configuration to be discussed next is much more appropriate. The noninverting design uses low value resistors for its gain determining network, hence circumvents the bandwidth problem at the same time as achieving high input impedance.

However, the inverting circuit does have an advantage over the noninverting arrange-

ment, because it operates with one input terminal grounded, thereby enabling a chopper stabilized amplifier to be used for utmost long-term stability. A further point is that the inverting configuration obviates any possibility of common mode errors and can operate, in theory at least*, with inputs in the thousands-of-volts range. The major pros and cons of the inverting circuit are summarized in Table 1.

NONINVERTING CONFIGURATION

The noninverting amplifier, Figure 2, achieves very high "bootstrapped" input impedance by opposing the input signal V_s with feedback V_f almost equal in magnitude to the input signal. The amplifier's net differential drive signal, represented as error voltage V_e in Figure 2, is then equal to the difference between input and feedback voltages, and may be a matter of millivolts...or even microvolts...for high gain amplifiers. Consequently, with only millivolts across the amplifier's differential input resistance R_{IN}, the signal current drawn from the signal source will also be proportionately small, giving the effect of artificially boosted input impedance. So far as the signal source is concerned, the amplifier draws an input current of only $(V_s-V_f)/R_{IN}$, rather than V_s/R_{IN}, and input resistance is raised from R_{IN} to approximately $AR_{IN} \times R_2/(R_1 + R_2)$, as Figure 2 demonstrates. More accurately, input impedance becomes $R_{IN}(1 + A\beta)$ in parallel with R_{cm}, where β is the feedback fraction $R_2/(R_1 + R_2)$, and R_{cm} is the common mode input resistance, or resistance from input terminal to ground.

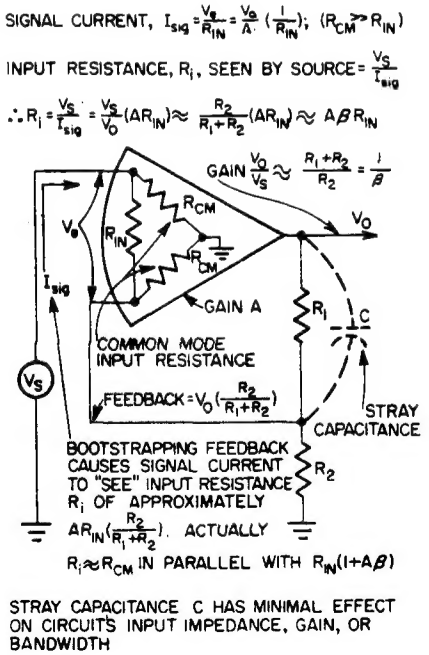


Fig. 2 - Noninverting circuit uses feedback to bootstrap input impedance, provides high gain without compromising bandwidth. Circuit is susceptible to common-mode error, and input voltage range is less than unit's supply voltage.

*A forthcoming Analog Dialogue article will show how a solid state op amp can be used to measure the voltage of a 10,000 volt DC supply with better than 0.1% accuracy.

Taking a typical example of an op amp with 10^6 open loop gain, 1 megohm input resistance, and connected in a noninverting circuit with closed loop gain, $(1/\beta)$, of 50, the bootstrapped input resistance R_I is 1 megohm x $(1 + 10^6/50)$ = 20,000 megohms. Frequently, the artificially increased input resistance is far higher than the amplifier's common mode input resistance, R_{cm}, or resistance from input to ground. Consequently, the common mode input resistance, rather than the bootstrapped differential input resistance, sets the ultimate limit on source loading effects. Nevertheless, an operational amplifier with 1 megohm differential input resistance frequently has a common mode input resistance of 1000 megohms, so that the noninverting configuration truly does make a high input resistance amplifier.

STRAY'S DON'T LIMIT BANDWIDTH

Although the gain-setting resistors R_1 and R_2 are shunted by leakage capacitance as before, the noninverting circuit's bandwidth limitation is by no means as severe as the inverting circuit's. This is because the noninverting amplifier's bootstrapped input resistance is independent of actual feedback resistance values, but instead, depends upon their resistance ratios. Actual input resistance, as Fig. 2 shows, is $R_I = R_{IN}(1 + A\beta)$ paralleled by the common mode input resistance R_{cm}. Consequently, closed loop gain $1/\beta = (R_1 + R_2)/R_2$, can be made arbitrarily high without actually using high resistance values.

For example, the amplifier discussed earlier could produce a closed loop gain, $1/\beta = (R_1 + R_2)/R_2$, of 1000 simply by using R_1 = 999 ohms and R_2 = 1 ohm. If the amplifier's open loop gain A was 10^6, input resistance would be raised by a factor of $(1 + 10^6/10^3)$, or 1000 fold, but the effect of the 1pf stray capacitance shunting the 999-ohm R_1 would be negligible. In practice, the values of R_1 and R_2 are decided on the basis of the amplifier's ability to supply enough current to excite them without depriving the external circuit of its load current. A typical amplifier's output rating is ±10 volt, 5mA, so that if 4mA were reserved for the load circuit, then the minimum value for $(R_1 + R_2)$ would be 10V/1mA = 10,000 ohms. Therefore, R_1 and R_2 become 9,990 ohms and 10 ohms respectively. Even so, the 1pf leakage does not begin to roll-off the closed loop gain much below $f_c = 1/2\pi 10^4 \times 10^{-12}$ = 15MHz. Internal amplifier response limitations are much more likely to set performance levels than external capacitance strays.

COMMON MODE ERROR

Despite the noninverting circuit's freedom from the effects of capacitance strays, it nevertheless is susceptible to a set of problems not encountered in the inverting amplifier. These are the common mode errors caused by unequal gains "behind" the amplifier's inverting and noninverting terminals, Figure 3A. Later, as we shall see, the external circuit, as well as an amplifier, creates common mode problems. In fact, the common mode errors, or rather the design measures adopted to overcome them, account for a large proportion of the price difference between operational amplifiers and high performance data amplifiers.

Although the transistors used in an operational amplifier are elaborately matched, and gain-stabilized by internal feedback, there may nevertheless be a gain difference between inverting and noninverting channels of 1 part in 10,000, or 0.01%, even for quite expensive units. In fact, run-of-the-mill FET op amps tend to have gain mismatches of 0.1%, and require considerable design ingenuity (as evidenced in high performance Model 147) to achieve gain equality of 0.0003%.

An example illustrates the problem. Consider an amplifier with a nominal open loop gain of 10,000 (very low for an op amp), and with 1 part in 10,000 gain error between inverting and noninverting signal channels. That is, the noninverting gain might be 10,000 while the inverting gain is only 9,999. If both input terminals are connected to a 10 volt common mode source, Figure 3B, the noninverting terminal can be imagined to create an output of 10 x 10,000 volts while the inverting terminal produces -

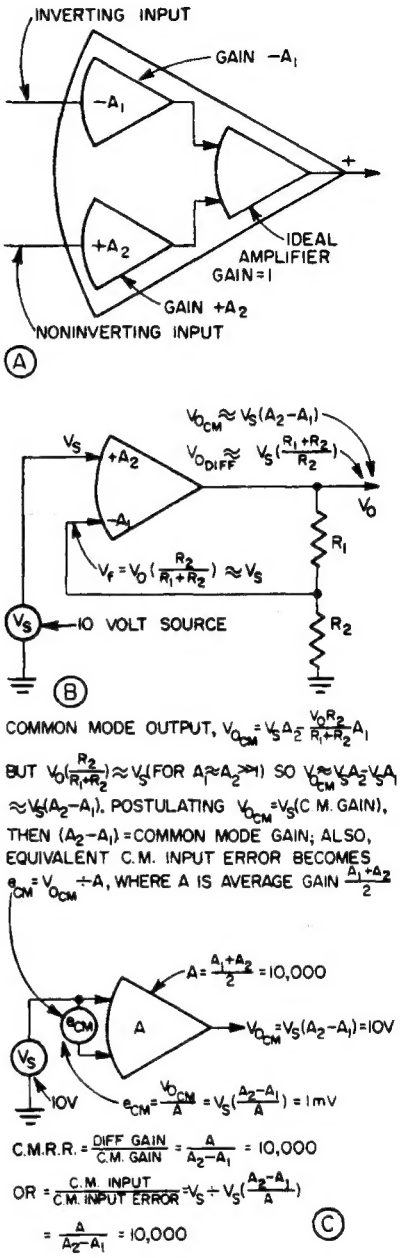


Fig. 3 - Unequal inverting and noninverting gains is basis for common mode error (A), creating common mode output proportional to gain inequality (B). Common mode output can be imagined to have been caused by differential component of common mode input, e_{cm}, which is applied between amplifier's input terminals (C). Value of hypothetical error source e_{cm} is common mode voltage divided by CMRR.

10 x 9999 volts. The net effect is an output of 10(10,000 - 9999), which is 10 volts. In other words, the common mode output $V_{o_{cm}}$ may be represented by $V_{cm}(A_2 - A_1)$, which for an ideal amplifier would be zero, but for the amplifier cited is 10 volts.

The factor $(A_2 - A_1)$ is termed the common mode gain G_{cm}. This is because the 10 volt common mode output may be regarded as having been produced by multiplying the common mode input voltage (10 volts) by this imaginary common mode gain: $V_{o_{cm}} = V_{cm} \times G_{cm}$. Complete circuits, as well as operational amplifiers themselves, may exhibit a common mode gain. In fact, even though a circuit is based on an (ideal) op amp with identical inverting and noninverting gains, it can develop a common mode error when unequal proportions of common mode voltage are applied to its inverting and noninverting terminals. Common mode <u>circuit</u> errors will be discussed after we have reviewed common mode <u>amplifier</u> errors in more detail.

COMMON MODE REJECTION RATIO

Amplifiers (and circuits too) may have their response to common mode input voltage defined in terms of a Common Mode Rejection Ratio, or CMRR. This ratio is a measure of the amplifier's ability <u>not to respond</u> to the common mode voltage applied simultaneously to both input terminals. One definition of CMRR is Signal Gain/ Common Mode Gain. For a differential op amp this CMRR becomes $A/(A_2 - A_1)$, where A is the nominal open loop or signal gain value: $\frac{1}{2}(A_1 + A_2)$, while $(A_2 - A_1)$ is the common-mode gain. A circuit's overall CMRR involves the amplifier's internal gain inequality, but also depends upon the amplifier's common mode input resistance, and upon deviations in external resistors from their calculated values.

It is worth noting that the CMRR, $A/(A_2 - A_1)$, is the inverse of the amplifier's fractional gain error, $(A_2 - A_1)/A$. The amplifier cited earlier, Fig. 3C, had a gain error of 1 part in 10,000, which leads automatically to a CMRR of 10,000.

Another way of viewing the common mode rejection ratio is to regard it as the ratio between the actual common mode voltage applied to both input terminals, V_{cm}, and a hypothetical common mode error signal e_{cm} that would create the same value of common mode output error when amplified along with true input signals. This imaginary common mode input error e_{cm} is then determined by dividing the actual common mode output error, $V_{cm}(A_2 - A_1)$, by the amplifier's normal mode signal gain A. (Where A is the average open loop gain $1/2\left(A_1 + A_2\right)$.

To use the amplifier cited earlier as an example, Figure 3C, its 10 volt common mode output voltage may be imagined to have been created by an equivalent common mode input error, e_{cm}, of 10 volts/10,000, or 1mV. The CMRR is now the ratio of the actual common mode output voltage (10 volts), to the differential component, e_{cm}, of the common mode input that would produce this same common mode output when multiplied by 10,000. This works out to 10/0.001 = 10,000, which, as one might expect is the same value as before.

PERCENTAGE CM ERROR

The percentage common mode output error for a given amplifier, or for a circuit, is the fraction (Error Output/ True Output) x 100%. If both error and true output are divided by the amplifier's gain, then the percentage error may also be referred to the input as the ratio: (Error Input/ True Input) x 100%.

Knowledge of an op amp's CMRR quickly leads to a value for the equivalent common mode input error, because one definition of CMRR is V_{cm}/e_{cm}. In other words, the differential error component of common mode input, e_{cm}, is $V_{cm}/CMRR$.

Percentage error may now be calculated from $100\% \times e_{cm}/V_s = 100\% \times V_{cm}/CMRR \doteq V_s$. If the amplifier already discussed, with 10 volt CM input and 10,000 CMRR, is used to measure 100mV signals, the ratio of equivalent CM input error to true input signal is $(10/10{,}000 \div 0.1) \times 100\% = 1\%$. Errors due to drift, source loading, long term aging, and finite gain must be added to the common mode error for a true statement of circuit performance.

The discussion thus far has been concerned largely with an amplifier's internal common mode error. We also pointed out that a circuit, as well as an amplifier, can develop common mode errors. However, the noninverting circuit, Fig. 3, is one particular configuration in which the voltage applied to the two amplifier terminals is simultaneously the common mode voltage and the signal voltage. (Note: $V_s \approx V_f$). Consequently, the common mode error and CMRR of the noninverting circuit is the same as the amplifier upon which the circuit is based, namely, $A/(A_2 - A_1)$. This point is considered further in Figure 6 on page 12.

NONINVERTING CIRCUIT'S VOLTAGE LIMITATION

The noninverting amplifier's input voltage capability is certainly no greater, and

generally less, than the voltage of the plus and minus supply lines. This limits a noninverting amplifier operating from a ±15 volt DC supply to a maximum input voltage level of less than ±15 volts. In many applications this may be a severe restriction... and one that drives the engineer to the inverting circuit even though he would like to take advantage of the noninverting configuration's high input impedance.

Table 1 compares the pros and cons of the noninverting circuit with those of the inverting configuration discussed previously. The next section will examine some of the pros and cons of differential amplifier circuits.

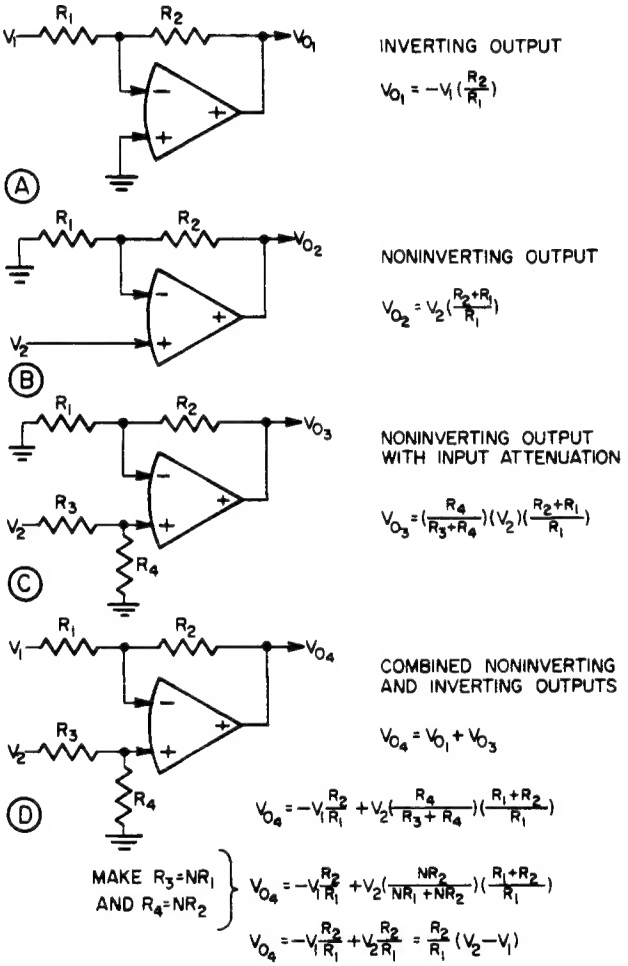


Fig. 4 - One-amplifier differential circuit combines inverting and noninverting operation. Arrangement is economical, but tends to exhibit worst features of the two circuits upon which it is based. Also, gain is difficult to vary without introducing common mode errors.

ONE-AMPLIFIER DIFFERENTIAL CIRCUIT

The evolution of a single op amp differential circuit from the inverting and noninverting configurations is shown successively in Figures 4A through 4D. This is a widely used differential design owing to its component economy. However, this very

economy is paid for at the price of inevitable compromises necessary in combining inverting and noninverting operation in a single amplifier circuit.

Instead of yielding the best features of the inverting and noninverting designs, the differential amplifier of Figure 4 suffers mainly from the disadvantages of both.

For example, the advantages of the inverting amplifier, as summarized in Table 1, include immunity from common mode errors, ability to operate from high input voltage, and ease of design with chopper stabilized amplifiers. All of these merits are sacrificed in the differential arrangement. Likewise, the advantages of the noninverting amplifier, which include ultra-high input impedance, immunity to bandwidth limitations, and ease in producing high gain, are lost in the differential circuit too.

However, the single amplifier differential configuration does have one edge, aside from economy, over the more sophisticated versions based on two or more separate op amps. Use of two amplifiers means in the worst case, twice the drift, noise and amplifier common mode errors, in addition to all the problems created by component tolerance errors. The single amplifier circuit, at least, contributes only one set of amplifier errors.

CIRCUIT COMMON MODE ERRORS

We have seen, in the section on noninverting circuits, how an amplifier's lack of perfect equality between inverting and noninverting gains creates a spurious output when a common mode voltage is applied to both input terminals. Now we will investigate a further and separate common mode problem that can occur in a circuit, regardless of whether the amplifier's internal gain characteristics are ideal.

The differential configuration, redrawn in Figure 5A, relies on the voltage divider effects $R_2/(R_1 + R_2)$ and $R_4/(R_3 + R_4)$ to apply equal fractions of the common mode voltage to the amplifier's inverting and noninverting terminals. So long as these fractions are identical, as theoretically they will be for the ideal circuit of Figure 4, then no differential component of common mode voltage will be created and the amplifier will develop zero common mode output. (This assumes a perfect amplifier in which $A_1 = A_2$).

But suppose ordinary off-the-shelf resistors with 0.1% tolerance are used for R_1, R_2, R_3 and R_4: then one can visualize a distribution of resistance in errors, which, in the worst case, make $R_4/(R_3 + R_4)$ larger than its theoretical value, while $R_1/(R_1+R_2)$ is smaller than this same ideal value. Now, of course, there will be a net fraction of common mode voltage e_{cm} applied differentially between the amplifier's input terminals, which will be amplified by noninverting gain factor of $(R_1 + R_2)/R_1$ to create a common mode output voltage error proportional to the resistance tolerances.

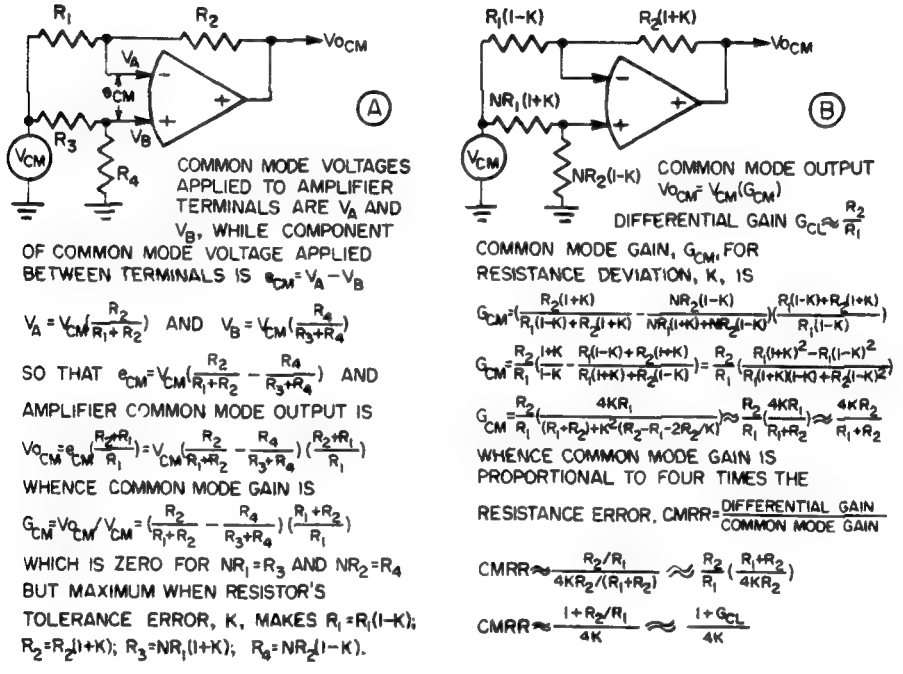


Fig. 5 - Unequal proportions of common mode voltage V_{cm} are applied to amplifier's inverting and noninverting terminals when external resistors deviate from their assigned values (A). Analysis shows that worst-case common mode error is proportional to four times the resistor tolerance fraction K, and that CMRR improves with closed-loop gain (B).

The worst-case distribution of resistance errors occurs when the four feedback resistors assume new values of $R_1(1 - K)$, $R_2(1 + K)$, $NR_1(1 + K)$, and $NR_2(1 - K)$, where K is the resistor tolerance specified by the resistor manufacturer. This arrangement is shown in Figure 5B, and its accompanying analysis demonstrates that the worst-case common mode gain is proportional to four times the resistance error K.

The circuit's common mode rejection ratio is defined as the ratio of closed loop, or normal mode gain, $G_{cl} = R_2/R_1$, to the common mode gain, $G_{cm} = 4KR_2/(R_1 + R_2)$. Thus, CMRR for the single amplifier circuit of Figure 5 becomes $(1 + R_2/R_1)/4K$.

However, the circuit's differential gain, R_2/R_1 appears explicitly in this CMRR expression, which may now be rewritten as $(1 + G_{cl})/4K$. In short, the circuit's CMRR improves with closed loop gain, but falls inversely with resistor tolerance error K.

ERROR EXAMPLE

In a practical instance based on a circuit using 0.1% resistors and operating at a closed loop gain R_2/R_1 of 100, the CMRR becomes (1 + 100)/4 x 0.1%. This works out to approximately 25,000 : 1.

If the same circuit measures a 100mV signal superimposed on a 10 volt common mode level, then the common mode error would be 100% x 10V/25,000 ÷ 100 mV, which gives a common mode error of 0.4%.

But this analysis accounts only for the common mode error due to imperfect resistors, Additionally, the amplifier's internal gain inequality contributes a second source of common mode error, which in the worst case must be added to the error caused by resistor tolerance.

The amplifier's internal gain, $(A_2 - A_1)$, and $CMRR_A = A/(A_2 - A_1)$, apply equally to the amplifier itself, and to the differential circuit in which the amplifier is connected, as Figure 6 shows. Accordingly, if the specification sheet shows the amplifier's CMRR to be 25,000, the additional common mode error in measuring 100 millivolts superimposed on the 10 volt common mode level is

100% x 10V/25,000 ÷ 100 mV.

This is an error of 0.4%.

Thus, in the worst case, where the common mode errors caused by external resistance deviation and by amplifier gain-inequality act in unison, the total common mode error adds up to 0.4% + 0.4% = 0.8%.

In general, the overall CMRR due to these

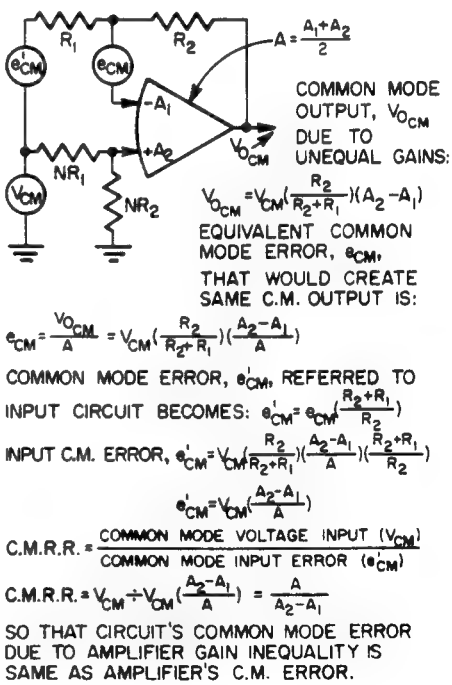


Fig. 6 - Amplifier's internal common mode error due to gain inequality reflects a CMRR to the circuit's input that is equal to that amplifier's own CMRR: $A/(A_2 - A_1)$.

separate causes is calculated in the same way that the net resistance of two parallel branches is calculated:

$$\text{Total CMRR} = \frac{\text{CMRR}_R \times \text{CMRR}_A}{\text{CMRR}_R + \text{CMRR}_A}$$

where CMRR_R and CMRR_A are the separate values for resistance and gain errors, respectively.

A useful design trick is to trim the external resistors so that the resulting common mode gain has opposite polarity to the common mode gain caused by the amplifier's unequal inverting and noninverting gains. This technique, for example, can give CMRR_R a negative value while CMRR_A is positive. The net effect is to create zero common mode output, and hence achieve infinite CMRR. The same result may be inferred from the equation for overall CMRR, above, since the denominator in this expression, $\text{CMRR}_R \pm \text{CMRR}_A$, is reduced to zero.

In a practical instance, and especially for transistor rather than FET-input amplifiers, this method can tweak-up the overall CMRR by a factor ranging from ten to perhaps one hundred.

However, there are several hazards to the technique. For example, if the external resistors drift away from their "tweaked-up" values, either through temperature instability or aging, then the amplifier's common mode compensation drifts away too. Similarly, the compensating method depends upon the constancy of the amplifier's internal CMRR, but in actuality, this parameter varies in response to several factors. For example, CMRR_A, changes with the amplitude of applied common mode voltage; it also varies with output loading and common mode frequency, and follows the long-term aging of internal resistors and semiconductors.

Consequently, the designer should become quite familiar with the amplifier's common mode characterisics, and should also make sure that his external resistors have long-term and temperature-induced drift characteristics commensurate with his accuracy needs.

GAIN CHANGE CREATES CM ERROR

We have seen how resistance deviations in a differential circuit's feedback components produce common mode error. In practice, it is possible to "tweak up" a differential amplifier for near-perfect circuit CMRR by making one or another of the resis-

tors slightly variable....or adding a small amount of trimming resistance in series or parallel. However, trouble really sets in when one wants to build a variable gain differential amplifier. If the circuit of Figure 5A uses 0.01% resistors for high CMRR, it would be exceedingly difficult to replace R_2 and R_4 with a ganged pair of variable resistors and still secure the same CMRR owing to the impossibility of maintaining good tracking between R_2 and R_4. Careful common mode trimming would come "untweaked". Accordingly, it is difficult and not entirely straightforward to build a variable gain differential amplifier capable of high CMRR.

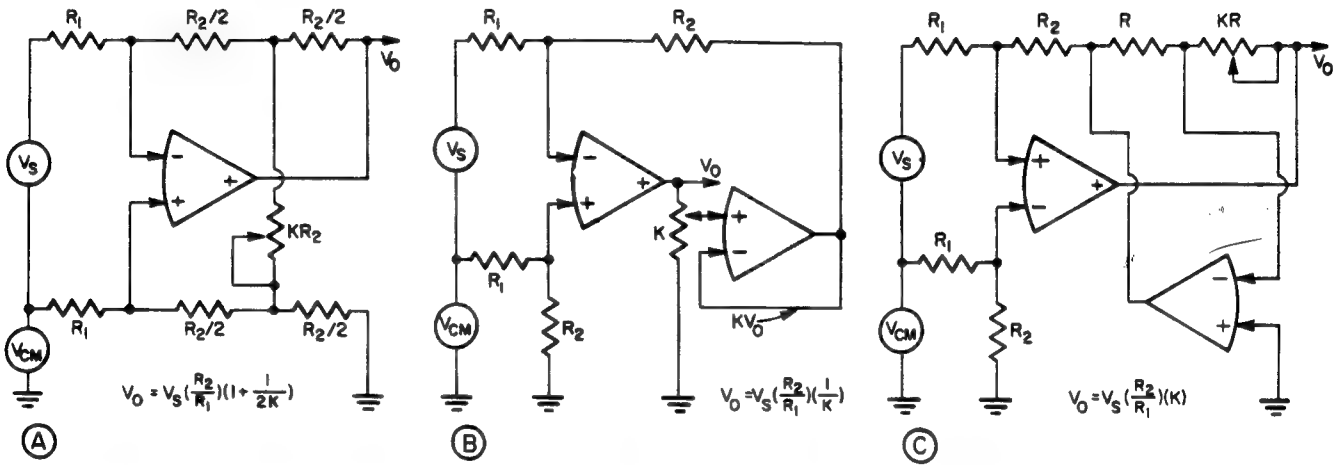


Fig. 7 - Circuit (A) uses single resistor to adjust gain without altering common mode balance, but requires six high-stability resistors in feedback circuit. Also, gain varies nonlinearly with K. Circuit (B) uses only four feedback resistors, but requires an auxiliary amplifier for 'unloading' resistor K. Gain also varies nonlinearly with K. Circuit (C) provides linear gain variation with aid of auxiliary amplifier, uses five fixed feedback resistors.

Various methods have been adopted for altering a differential amplifier circuit's gain using a single variable resistor, instead of the ganged pairs of resistors required by the circuit of Figure 5 on page 11. Some of these are presented in Figure 7 along with their closed loop gain equations. One problem with such circuits is their lack of gain linearity as a function of the gain adjusting resistance, although this problem can be overcome by use of an inexpensive auxiliary amplifier, as shown by the circuit on the right.

CM ERRORS DUE TO AMPLIFIER INPUT RESISTANCE

Yet a further source of common mode error is the unbalancing effect of the amplifier's own common mode input resistance R_{cm}. Because the common mode resistances between the inverting and noninverting terminals and ground are, in effect, placed in parallel with feedback resistors R_2 and R_4 of Fig. 5, they modify the fractions of common mode

voltage applied to the two input terminals. So long as these resistances are equal, they will have no effect on the CMRR. However, they are never identical in reality, and so add to the common mode errors already created by resistor tolerances and amplifier internal gain differences.

Errors due to common mode resistance are minimized not so much by ensuring that the two resistance values are equal, but in selecting resistors R_2 and R_4 that are small compared to the nominal R_{cm} value. Or working the other way around, by selecting an amplifier with very high common mode input resistance. An example of such an amplifier is the FET or varactor bridge type, while even the recently developed high performance differential transistor amplifiers feature 10^9 ohm common mode impedance. Errors due to thousand-megohm R_{cm} values shunting 100 kilohm feedback resistances (R_2 and R_4) amount to only about 0.01% net resistance deviation. Further, because both R_2 and R_4 are simultaneously shunted by virtually-equal common mode values, the net unbalancing effect will be negligible compared with other error sources.

We now see that any given single-amplifier differential circuit is susceptible to common mode errors from at least three distinct sources, namely, internal gain inequality, feedback resistor tolerances, and the shunting effect of the amplifier's common mode input resistance.

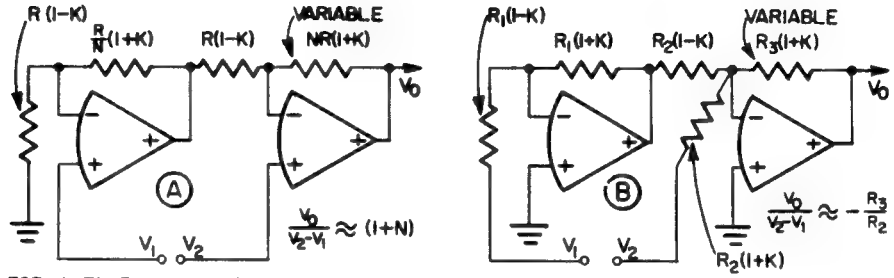
In addition, a fourth source of error can crop up when even the most perfect differential amplifier is connected into a practical measuring circuit. This is error caused by unbalanced source resistance, and which is dealt with in Figure 15 and its associated discussion.

FURTHER DIFFERENTIAL CIRCUITS

It is possible to improve on the single amplifier circuit in various ways by developing a differential configuration around two separate op amps instead of one. Off-the-cuff, one might suppose that a differential design based on two noninverting amplifiers would benefit from the noninverting circuit's high input impedance and relative immunity to capacitance strays. Likewise, a differential circuit based on two inverting amplifiers can be envisaged to handle very high levels of common mode input voltage and afford immunity to the op amp's internal common mode errors.

Two such circuits, based on noninverting amplifiers, are analyzed in Figure 8, and

their major features included in Table 1. It is worth observing that the common mode error due to external resistance deviations decreases with closed loop gain for the noninverting circuit, whereas the inverting configuration's CMRR is constant. Offsetting this advantage of the noninverting design is its additional error caused by gain inequalities within the two amplifiers. Closed loop gain of both Figure 8A and Figure 8B can be varied in proportion to the output amplifier's feedback resistor.



FOR OUTPUT DUE TO V_1 INPUT

$$V_{O_1} = -V_1\left(\frac{\frac{R}{N}(I+K)+R(I-K)}{R(I-K)}\right)\left(\frac{NR(I+K)}{R(I-K)}\right) = -V_1\left(\frac{R+NR}{R}\right) \text{ WHEN } K=0$$

FOR OUTPUT DUE TO V_2 INPUT

$$V_{O_2} = V_2\left(\frac{NR(I+K)+R(I-K)}{R(I-K)}\right) = V_2\left(\frac{R+NR}{R}\right) \text{ WHEN } K=0$$

NET OUTPUT, $V_{O_1}+V_{O_2}$ FOR $K=0 = (I+N)(V_2-V_1)$

DIFFERENTIAL GAIN $\frac{V_O}{V_2-V_1} = (I+N) = G_{CL}$

FOR OUTPUT DUE TO V_1 INPUT

$$V_{O_1} = V_1\left(\frac{R_1(I+K)}{R_1(I-K)}\right)\left(\frac{R_3(I+K)}{R_2(I-K)}\right) = V_1\left(\frac{R_3}{R_2}\right) \text{ WHEN } K=0$$

FOR OUTPUT DUE TO V_2 INPUT

$$V_{O_2} = -V_2\left(\frac{R_3(I+K)}{R_2(I+K)}\right) = -V_2\left(\frac{R_3}{R_2}\right) \text{ WHEN } K=0$$

NET OUTPUT, $V_{O_1}+V_{O_2}$ FOR $K=0 = \frac{R_3}{R_2}(V_1-V_2)$

DIFFERENTIAL GAIN $\frac{V_O}{V_2-V_1} = -\frac{R_3}{R_2} = G_{CL}$

BOTH CIRCUITS DEVELOP COMMON MODE OUTPUT $V_{O_{CM}}$ WHEN FRACTIONAL RESISTANCE DEVIATION IS K, AND $V_1 = V_2 = V_{CM}$

$$V_{O_{CM}} = V_{CM}\left[\frac{NR(I+K)+R(I-K)}{R(I-K)} - \left(\frac{\frac{R}{N}(I+K)+R(I-K)}{R(I-K)}\right)\left(\frac{NR(I+K)}{R(I-K)}\right)\right]$$

$$V_{O_{CM}} = V_{CM}\left(\frac{N(I+K)+(I-K)}{I-K} - \frac{(I+K)^2+N(I+K)(I-K)}{(I-K)^2}\right)$$

$$V_{O_{CM}} = V_{CM}\left(I+\frac{N(I+K)}{I-K} - \frac{(I+K)^2}{(I-K)^2}\frac{N(I+K)}{I-K}\right) = V_{CM}\left(\frac{(I-K)^2-(I+K)^2}{(I-K)^2}\right)$$

$$V_{O_{CM}} \approx -V_{CM}(4K)$$

COMMON MODE GAIN = 4K

$$\text{CMRR} = \frac{\text{DIFF GAIN}}{\text{C.M. GAIN}} = \frac{I+N}{4K} = \frac{G_{CL}}{4K}$$

$$V_{O_{CM}} = V_{CM}\left[\left(\frac{I+K}{I-K}\right)\left(\frac{R_3(I+K)}{R_2(I-K)}\right) - \frac{R_3(I+K)}{R_2(I+K)}\right]$$

$$V_{O_{CM}} = V_{CM}\left(\frac{(I+K)^2}{(I-K)^2} - \frac{I+K}{I+K}\right)\left(\frac{R_3}{R_2}\right)$$

$$V_{O_{CM}} = V_{CM}\left(\frac{(I+K)^2}{(I-K)^2} - I\right)\left(\frac{R_3}{R_2}\right) = V_{CM}\left(\frac{(I+K)^2-(I-K)^2}{(I-K)^2}\right)\left(\frac{R_3}{R_2}\right)$$

$$V_{O_{CM}} \approx V_{CM}\left(4K\frac{R_3}{R_2}\right) \quad \text{NOTE } \frac{R_3}{R_2} = G_{CL}$$

COMMON MODE GAIN = $4KG_{CL}$

$$\text{CMRR} = \frac{\text{DIFF GAIN}}{\text{C.M. GAIN}} = \frac{R_3/R_2}{4KR_3/R_2} = \frac{I}{4K}$$

Fig. 8 - Use of two noninverting amplifiers gives differential circuit high input impedance, and CMRR that improves with closed loop gain. However, circuit is susceptible to amplifier's internal common mode errors, has limited input voltage range, and requires isolated power supplies when based on chopper stabilized amplifiers (A).

Alternative circuit uses two inverting amplifiers, has constant CMRR for external resistance deviations, handles high input voltage levels, is immune to common mode error of individual amplifiers, and can be based on chopper stabilized amplifiers without needing special power supplies. However, input resistance is limited to the value used for R_1 (B).

ERROR CANCELLING CONFIGURATION

The differential amplifier of Figure 9 has the unusual attribute of providing theoretical immunity to common mode errors caused by resistance deviations. (Errors due

to gain inequality within the two amplifiers remain, however.)

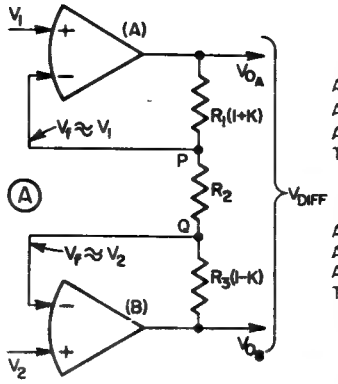
The error analysis, Figure 9B, shows that the circuit has unity common mode gain when the two amplifiers are considered separately, but because both amplifiers feature this same unity common mode gain, the common mode output measured BETWEEN the output terminals is theoretically zero. This means that the common mode differential gain is also zero, and the circuit's common mode rejection ratio theoretically infinite, insofar as resistance errors are concerned.

Galvonometers, relays, coils and other isolated loads can be driven directly from the push-pull output with near-perfect immunity to resistor-induced common mode errors. On the other hand, an additional stage of differential amplification is required for single ended loads.

Figure 10 shows the error cancelling circuit followed by a differential-to-single-ended "interface" amplifier. Overall gain of the two cascaded stages is then

Gain (A) x Gain (B)

and the total CMRR reduces to



AMPLIFIER (A) INPUTS ARE: $-V_1$ APPLIED DIRECTLY TO (+) TERMINAL AND V_2 APPLIED AT POINT Q THEN FED TO (−) TERMINAL

AMPLIFIER (B) INPUTS ARE: $-V_2$ APPLIED DIRECTLY TO (+) TERMINAL AND V_1 APPLIED AT POINT P THEN FED TO (−) TERMINAL

AMPLIFIER (A) OUTPUT IS SUM OF OUTPUTS DUE TO V_1 AND V_2

$$V_{O_A} = V_{O_{A(V_1)}} + V_{O_{A(V_2)}}$$

$$V_{O_{A(V_1)}} = V_1\left(\frac{R_1(1+K)+R_2}{R_2}\right);\quad V_{O_{A(V_2)}} = -V_2\left(\frac{R_1(1+K)}{R_2}\right)$$

$$V_{O_A} = V_1\left(\frac{R_1(1+K)+R_2}{R_2}\right) - V_2\left(\frac{R_1(1+K)}{R_2}\right)$$

$$V_{O_A} = V_1 + \frac{R_1}{R_2}(1+K)(V_1 - V_2)$$

AMPLIFIER (B) OUTPUT IS SUM OF OUTPUTS DUE TO V_2 AND V_1

$$V_{O_B} = V_{O_{B(V_2)}} + V_{O_{B(V_1)}}$$

$$V_{O_{B(V_2)}} = V_2\left(\frac{R_3(1+K)+R_2}{R_2}\right);\quad V_{O_{B(V_1)}} = -V_1\left(\frac{R_3(1+K)}{R_2}\right)$$

$$V_{O_B} = V_2\left(\frac{R_3(1+K)+R_2}{R_2}\right) - V_1\left(\frac{R_3(1+K)}{R_2}\right)$$

$$V_{O_B} = V_2 + \frac{R_3}{R_2}(1-K)(V_2 - V_1)$$

CIRCUIT'S DIFFERENTIAL OUTPUT, $V_{DIFF} = V_{O_A} - V_{O_B}$

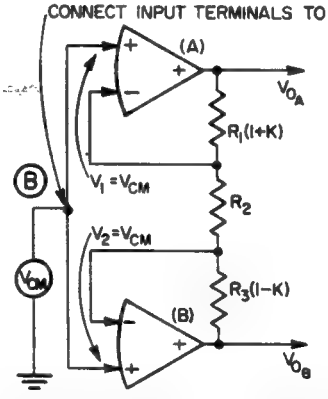
$$V_{DIFF} = \left[V_1 + \frac{R_1}{R_2}(1+K)(V_1 - V_2)\right] - \left[V_2 + \frac{R_3}{R_2}(1-K)(V_2 - V_1)\right] = (V_1 - V_2) + (V_1 - V_2)\left[\frac{R_1}{R_2}(1+K) + \frac{R_3}{R_2}(1-K)\right]$$

$$V_{DIFF} = (V_1 - V_2)\left(1 + \frac{R_1(1+K)}{R_2} + \frac{R_3(1-K)}{R_2}\right) = (V_1 - V_2)\left(1 + \frac{R_1+R_3}{R_2} + \frac{K(R_1 - R_3)}{R_2}\right)$$

AND IF K=0, $V_{DIFF} = (V_1 - V_2)\left(1 + \frac{R_1+R_3}{R_2}\right)$ SO THAT DIFFERENTIAL GAIN,

$$\frac{V_{DIFF}}{V_1 - V_2} = 1 + \frac{R_1+R_3}{R_2}$$

CONNECT INPUT TERMINALS TO COMMON MODE SOURCE, V_{CM}



$$V_{O_A} = V_1 + \frac{R_1(1+K)}{R_2}(V_1 - V_2)$$

BUT $V_1 = V_2 = V_{CM}$

SO $V_{O_A} = V_{CM}$

$$V_{O_B} = V_2 + \frac{R_3(1-K)}{R_2}(V_2 - V_1)$$

BUT $V_2 = V_1 = V_{CM}$

SO $V_{O_B} = V_{CM}$

COMMON MODE OUTPUT FOR INDIVIDUAL AMPLIFIERS IS V_{CM}, SO THAT COMMON MODE GAIN IS UNITY, REGARDLESS OF RESISTOR DEVIATIONS K. ALSO, THE DIFFERENTIAL COMPONENT OF COMMON MODE OUTPUT, $(V_{O_{A(CM)}} - V_{O_{B(CM)}}) = V_{CM} - V_{CM} = 0$, SO THAT THE DIFFERENTIAL C.M. GAIN IS ZERO. HENCE, CONSIDERING RESISTOR ERROR ONLY, THE CIRCUIT HAS A THEORETICALLY—INFINITE DIFFERENTIAL CMRR.

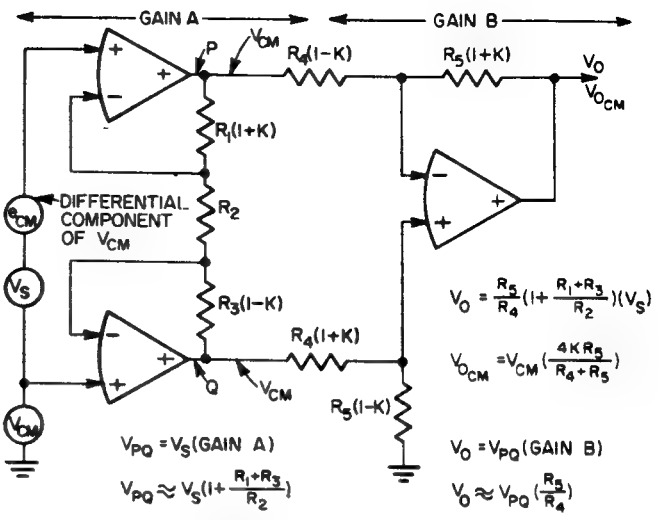
Fig. 9 - Differential circuit is immune to cc _on mode errors caused by resistance deviations, but remains susceptible to the amplifier's internal common mode errors. Circuit can be used to drive galvanometers, relays, magnetic coils, and other isolated loads, without need for conversion to single-ended output.

Gain (A)[1 + Gain (B)]/4K. A chart of the overall CMRR, Figure 10, suggests that the circuit's common mode performance can be maximized by assigning most of the gain to the first stage. In fact, fractional gain for the second stage appears to improve CMRR considerably.

Actually, this advantage cannot be pushed too far without running into another source of difficulty. Designing the first stage for high gain will either restrict the level of common mode voltage, or cramp the circuit's dynamic signal swing. Or both.

Because the individual amplifiers used in the first stage operate with unity common mode gain, output signals at points P and Q, Figure 10, vary around the common mode level, V_{cm}, of the input. If, for example, V_{cm} is 9.5 volts, and the amplifiers are built for a ±10 volt output rating, then the maximum output signal swing cannot be greater than 10-9.5 = 0.5 volts.

A circuit with 100:1 first-stage gain could not handle input signals larger than 0.5/100 = 5mV, without driving output (at P & Q) "into the



SECOND STAGE CONVERTS V_{CM} AT P AND Q INTO COMMON MODE OUTPUT $V_{O_{CM}} = V_{CM}(\frac{4KR_5}{R_4+R_5})$

DIFFERENTIAL COMPONENT OF V_{CM} AT INPUT, e_{CM}, IS C.M. OUTPUT DIVIDED BY OVERALL DIFFERENTIAL GAIN; $e_{CM} = V_{O_{CM}} \div [(\text{GAIN A})(\text{GAIN B})]$

$$e_{CM} = V_{CM}(\frac{4KR_5}{R_4+R_5}) \Big/ (1+\frac{R_1+R_3}{R_2})(\frac{R_5}{R_4}) = V_{CM}(\frac{4KR_5}{R_4+R_5})(\frac{R_4}{R_5})(\frac{1}{\text{GAIN A}})$$

GAIN A GAIN B

OVERALL CMRR $= \frac{V_{CM}}{e_{CM}}$

$$\text{CMRR} = V_{CM} \div (\frac{V_{CM}(\frac{4KR_5}{R_4+R_5})}{\text{GAIN A}})$$

$$\text{CMRR} = \frac{\text{GAIN A}}{4K}(1+\frac{R_5}{R_4})$$

$$\text{CMRR} = \frac{\text{GAIN A}}{4K}(1+\text{GAIN B})$$

(GAIN A)(GAIN B)=100		CMRR
GAIN A	GAIN B	$\frac{\text{GAIN A}}{4K}(1+\text{GAIN B})$
0.1	1000.0	100.1/4K
1.0	100.0	101/4K
10.0	10.0	110/4K
100.0	1.0	200/4K
1000.0	0.1	1100/4K

TABLE SHOWS THAT FIRST STAGE GAIN SHOULD BE HIGHEST FOR MAXIMUM C.M.R.R.

Fig. 10 - Right-hand differential stage develops single-ended output from push-pull input circuit. Arrangement provides high input impedance and allows low-value, high-tolerance resistors to be used for wide bandwidth and maximum CMRR. Chart shows advantage of having first stage contribute most of the gain.

Not revealed in drawing is the fact that the second stage's gain-inequality errors are reduced in proportion to first stage's normal-mode gain. (See Table I)

Disadvantage lies in the superimposition of output signals at P and Q onto the common mode voltage V_{cm}. This can cramp gain, or dynamic range, or both, because first stage's output signals, perched on high V_{cm} values, can drive amplifier into saturation.

stops". Large input signals could only be handled by using lower values of first-stage gain, or by reducing the common mode level upon which these signals are superimposed.

Table 1 summarizes the pros and cons of these differential circuits, and prepares the groundwork for developing a high-performance data aquisition circuit.

HANDLING LOW-LEVEL SIGNALS

Having established some of the key features for several standard op amp circuits, we are now in a position to investigate data measuring applications and learn how conventional op amps fit (or fail to fit), these requirements. We will also see why a data amplifier must almost invariably be a differential amplifier, even though the transducer itself generates a single-ended output.

Data amplifiers are widely used to measure low level signals developed by strain gauges, thermocouples, biological probes, and many other sensitive transducers. Very often, the transducer is located at a remote test site, while the amplifier is housed some distance away in an instrumentation building. For example, signals developed by strain gauges strung along a bridge structure would most probably be fed back to a data center at one end of the bridge. Similarly, thermocouple temperature signals developed during rocket engine testing would usually be fed to recorders and computers located in a well-protected blockhouse.

Separate sites for generating and measuring the data create the basic difficulties in accurate data acquisition. The trouble arises when both transducer and instrumentation are separately grounded. We shall explore this condition in due course. In the meanwhile, the topic of ground loops, which multiple grounds introduce, can best be demonstrated on the familiar territory of an ordinary Hi-Fi installation.

GROUND LOOPS IN A HI-FI

If the Hi-Fi signals are developed by a tape recorder, microphone and preamplifier, or other signal source with its own DC power supply, then fed to a main power amplifier, also powered by its own transformer and regulator, then the prospects for

trouble are well established.

A simple Hi-Fi system, Figure 11A, introduces the ground loop problem which occurs when signals must be transferred from one piece of equipment to another: in this case from microphone preamplifier to the output amplifier. The kernel of the ground loop problem lies in the 60Hz leakage current that flows between primary and secondary of both power transformers, and which is then converted into a 60Hz noise at the power amplifier's input circuit.

Dust and atmospheric humidity can reduce the leakage resistance between a transformer's primary and secondary windings to a few megohms; poor primary-to-secondary shielding can place a substantial leakage capacitance in parallel with the leakage resistance. For example, 100pf of leakage capacitance places roughly 30 megohms reactance in parallel with the leakage resistance. These leakage paths set up currents that circulate between both amplifiers, developing spurious hum voltages that are applied along with the signal to the output amplifier.

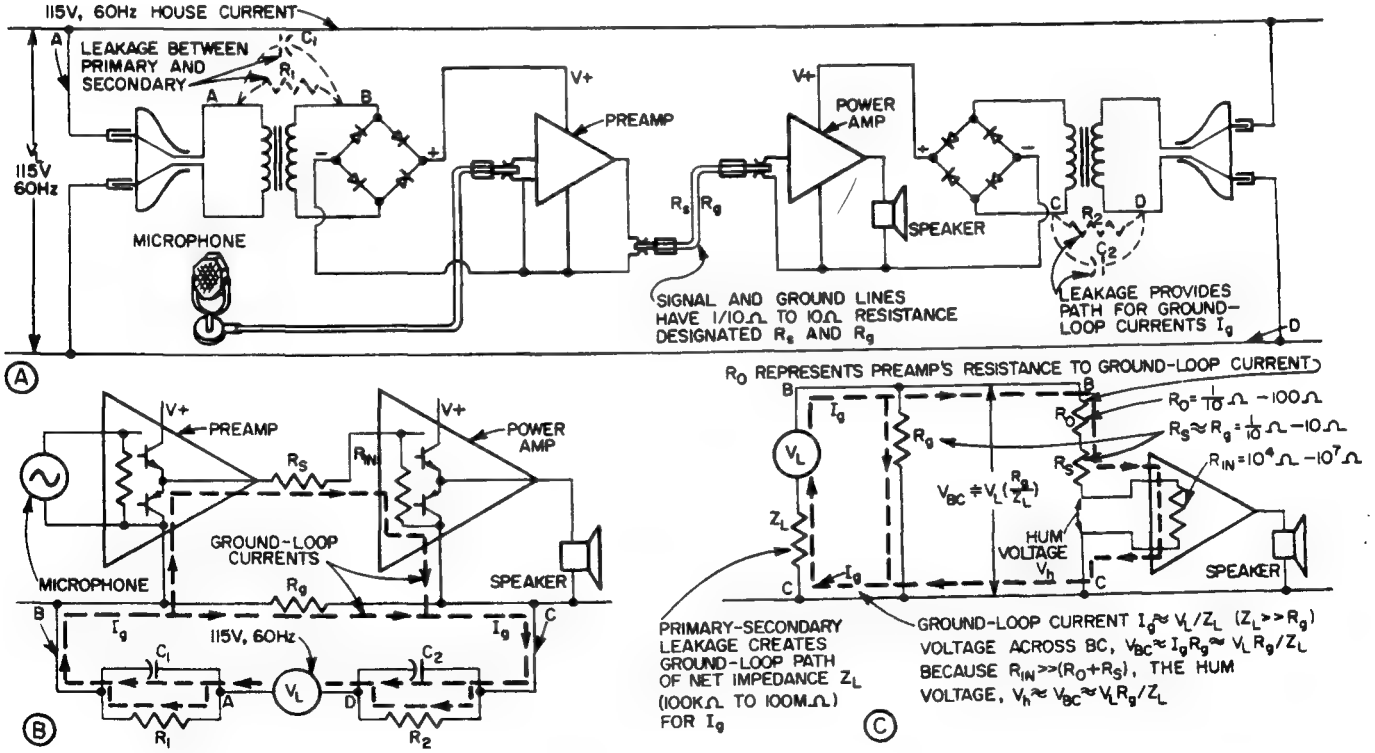


Fig. 11 - Transformer leakage sets up ground-loop current Ig that circulates between the two amplifiers via path ABCD (A). Ground-loop current flows through signal and ground lines connecting the two amplifiers (B), and creates hum voltage V_h at power amplifier's input terminals (C).

An equivalent circuit, Figure 11B, shows that the leakage currents flow in parallel through the ground and signal lines connecting both amplifiers (via the twin paths ABCD). Both these lines (which may be a coaxial cable in which the ground lead is the outer sheath), have a finite resistance, R_g and R_s, even though it may be as low as a fraction of an ohm. Actually, plug and socket interconnections can introduce appreciable resistance, especially if they are oxide-coated or loose-fitting.

A third diagram, Figure 11C, lumps the leakage resistance and reactance of both transformers into a composite leakage impedance Z_L connected in series with the 115 volt, 60Hz source designated V_L. If we assume that the leakage resistance and reactance of each transformer amount to about 5 megohms, then the two series-connected leakage impedances will total somewhat less than 10 megohms. Since transformer leakage is by far the largest impedance in the ground current path, the ground currents will be roughly equal to $V_L/Z_L \approx$ 115 volts/10 megohms. This leads to a nominal 11-microamp ground loop current that divides between the two parallel paths provided by R_g and the series-connected resistances, R_o, R_s, and R_{IN}.

Because the amplifier's input resistance R_{IN} will be very high compared to the ground-conductor's resistance R_g, most of the 11uA ground loop current will flow through R_g. Consequently, hum voltage developed across R_g will be 11uA x R_g. If the ground path (including plug-and-socket connections) has 1 ohm resistance, then the hum voltage V_{BC} across R_g will be 11uV. We can also express this voltage as a fraction of the 115 volt supply: $V_{BC} = V_L \times R_g/Z_L$.

Now we are in a position to determine the proportion of this 11uV hum voltage that is applied to the amplifier. Actually, most of it is. The hum voltage, V_{BC} developed across R_g is applied to the series network of R_o, R_s and R_{IN}, but because amplifier input resistance R_{IN} is usually orders-of-magnitude greater than R_o and R_s, almost the whole of the hum voltage is developed across R_{IN}. That is, hum voltage

$$V_h = V_{BC} \times R_{IN} / (R_{IN} + R_o + R_s) \approx V_{BC}.$$

Two obvious tactics for reducing hum present themselves. In the first place, the transformers should be "leakproof" so as to minimize ground loop currents. Secondly, the resistance R_g of the ground conductor should be made as low as possible in order

to "short circuit" the hum voltage between points B and C. Both these requirements suggest that one should buy a packaged Hi-Fi system for which a single manufacturer has taken overall "systems responsibility". Otherwise, it would be possible for different manufacturers of the various components to blame "the other guy" for the excessive ground-loop hum.

DATA MEASUREMENTS

The Hi-Fi system just described paves the way for understanding ground loop errors that occur in data measuring systems. We will see, for example, that one way to eliminate errors caused by earth voltages is to use a differential amplifier, even when measuring single ended signals. We will also see that the key specifications for a data amplifier include ultra-high common mode and differential input impedance, utmost common mode rejection ratio, high DC stability, and very often, wide bandwidth, fast slewing and fast settling.

It will also become evident as the argument proceeds, that all the performance specs for measuring millivolt signals developed by remote transducers are never simultaneously available in off-the-shelf operational amplifiers. Instead the data amplifier must be designed from the ground up and the key specs built right in at a price perhaps twice the cost of a premium op amp.

HYPOTHETICAL MEASUREMENT EXAMPLE

Figure 12A presents a hypothetical data measuring system that points up the sources of ground loop error occurring when signal source and data handling equipment are separately located, and grounded at both locations. In this instance, the signal is generated by a thermocouple placed in the stream of exhaust gases from a rocket motor undergoing test. The thermocouple feeds its signals over shielded cables to recording and data processing equipment located for safety in a blockhouse some 200 feet from the test site.

The fundamental data acquisition problem is caused by the separation of signal source and signal handling circuitry, both of which are invariably grounded (deliberately or otherwise), at the two different locations. The difference in potential between the

two geographically-separate ground points ends up as an error voltage applied to the amplifier along with its true input signals. The problem turns out to be closely analogous to the Hi-Fi ground loop difficulties already discussed.

EARTH POTENTIALS

One can well appreciate, to take an extreme example in New York City, that if one terminal of a sensitive voltmeter was connected to a ground plate in Times Square, and the other terminal connected to a ground plate in Grand Central Station, that there would be a substantial reading on the meter. Among the sources of potential difference between Times Square and Grand Central are the infinite variety of earth

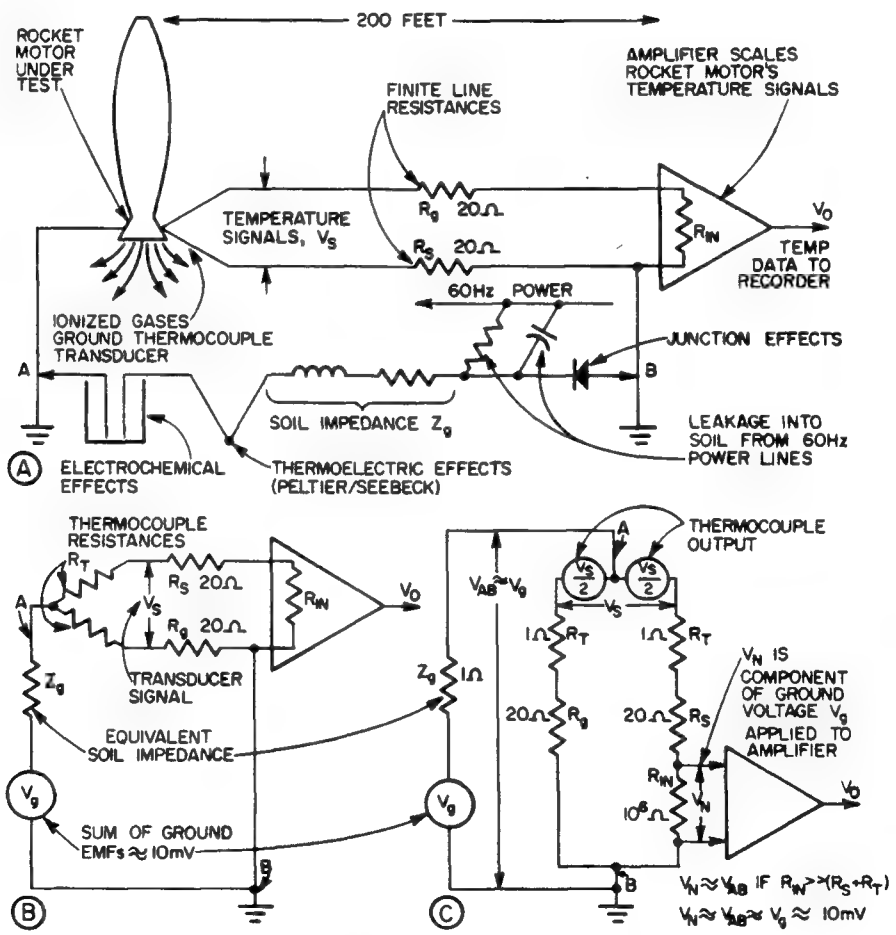


Fig. 12 - Separation of signal source and data amplifier can lead to considerable potential differences between ground connections at each location (A). Ground voltage, attaining 5 volts in extreme instances, is represented as V_g in series with ground impedance Z_g (B). Circulating "ground loop" current set up by V_g develops substantial error voltage V_N at amplifier's input terminals (C).

currents due to the city's telephone, electrical and subway services. Other contributors might be electrochemical and thermovoltaic (Seebeck) effects in the soil created by water and sewage services, and by minerals and building foundations. Currents created during lightning storms would add large transients effects too. On the whole, it wouldn't be surprising to find a large enough voltage difference between the two locations to energize a flashlight bulb, or even power a transistor radio for free.

If one now returns from New York City to the rocket test station of Figure 12, the ground voltages are still present, although their profusion of causes are less obvious. Nevertheless, in extreme instances the data systems designer has found that his signals are sitting upon as much as 5 volts of ground potential-difference. More typically, voltages from 1mV upwards are almost invariably present.

Figure 12A illustrates typical sources of ground potential between transducer and instrumentation sites. They include electrochemical effects (analogous to storage batteries), rectifier effects caused by soil crystals contacting buried metals and ores, thermoelectric effects created by temperature gradients in buried metals and soil elements, plus capacitive, inductive, and resistive coupling from power lines, charged clouds, and so forth. Doubtless there are many more.

Figure 12B lumps all these voltages together into a single ground EMF source V_g in series with the sum, Z_g, of all the ground impedances between rocket and blockhouse. As in the Hi-Fi example, it turns out that a substantial proportion of this ground voltage is developed across the amplifier's input terminals. Impedance levels now differ however. Whereas it would be rare to find the earth's resistance exceeding about 1 ohm, it is not unusual for 200 feet of connecting cables to introduce 20 ohms and upwards resistance in each line. Consequently, as shown in Figure 12C, practically the whole of the ground voltage (10mV) is applied across points A and B, and in turn across the amplifier's input terminals. Figure 12C shows the thermocouple transducer as a low resistance, designated $2R_T$, split between the two separate current paths joining A and B. (The thermocouple is represented for simplicity by resistance R_T in each ground loop path.)

ELIMINATING GROUND LOOP ERRORS

Before discussing the most practical and inexpensive method for eliminating ground potential errors, it helps fill in the picture by considering alternative approaches that are sometimes adopted.

Perhaps most obvious is some way of interrupting the continuity of the ground loop, but at the same time preserving the path for thermocouple signals. Referring to Figure 12C for example, one can see that increasing the value of ground impedance Z_g would be a step in the right direction. Perhaps a chemical poured into the ground? Another error-reducing stratagem would be to reduce the resistance of the ground conductor R_g so as to "short circuit" the ground potentials V_{AB}. This latter method is generally expensive, and anyway, the electronic method discussed in due course is far simpler than laying heavy ground conductors.

An alternative method, and one that is theoretically equivalent to raising ground resistance, is to break the ground current path, either by operating the amplifier from an isolated power supply, or by insulating the thermocouple from ground.

Neither of the methods are as simple as they appear. For instance, the amplifier is frequently used to feed signals into recorders, A-D converters, displays, and other data-handling equipment, all of which are themselves likely to be grounded. In this case, the ground-loop is completed through the amplifier thence to ground via the subsequent piece of equipment. Running the amplifier from an isolated supply is then useless.

Very often, it is necessary to weld the thermocouple to the structure being monitored, in order to secure utmost thermal conductivity. And even if this extreme measure is not required, the ionized gas issuing from the rocket motor of Figure 12 will certainly provide a low-resistance path from thermocouple to ground.

But even assuming that one or another of these measures is possible: there is yet a further phenomenon that couples either the transducer or the amplifier to ground, and this is leakage capacitance. The problem of minimizing the capacitance coupling between any part of the measuring circuit and ground is a major subject on its own, and

we can do little more than draw the reader's attention to the numerous papers cited in the bibliography at the end of this article.

In any event, the instrumentation engineer is frequently presented with a pair of wires carrying signal and ground loop noise, and has little opportunity to make large-scale modifications to the overall system. Instead, he must seek ways within his instrumentation package to reject the ground currents and consequent error voltages.

One well-known principle for interrupting the ground loop currents is to interpose an "open circuit" between signal source and amplifier, but arrange for the "open circuit"

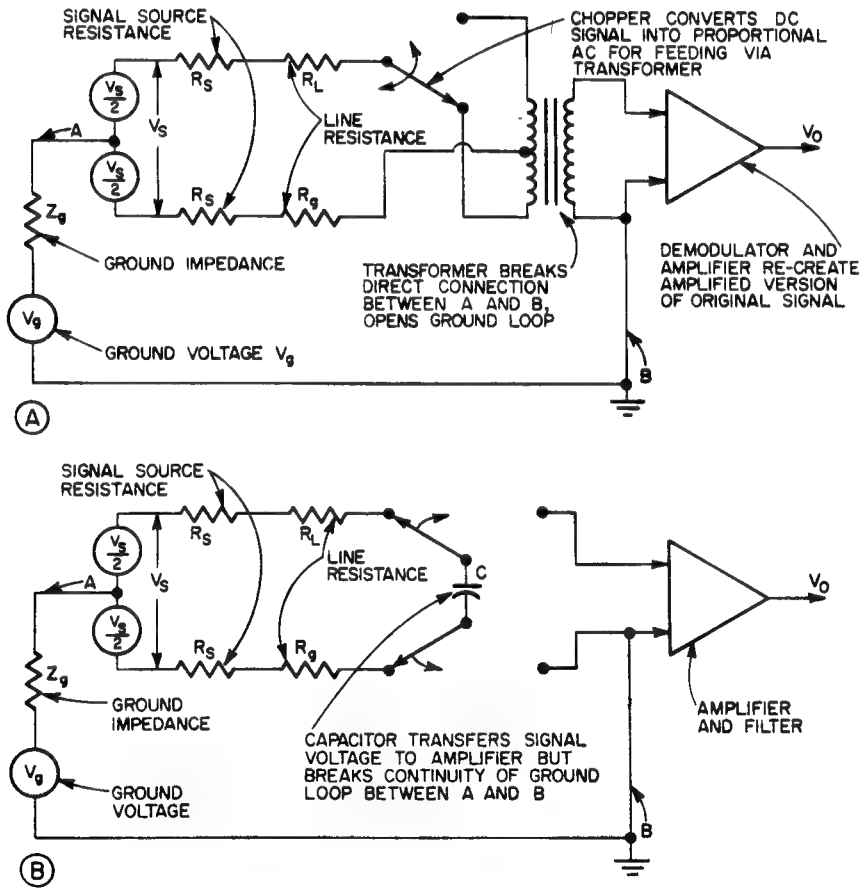


Fig. 13 - Magnetic coupling between transformer's primary and secondary breaks direct connection for ground-loop currents, transmits signal as equivalent AC voltage (A). Alternative technique breaks direct ground-loop continuity with switched capacitor that alternately charges to signal voltage V_s then passes this voltage to the amplifier (B).

to transmit signal currents while it blocks ground loop currents. This seemingly impossible task is accomplished by the "DC transformer" between thermocouple and final amplifier, as shown in Figure 13A. The transformer, which is actually a modulator-demodulator arrangement, responds (in principle at least) only to signal voltage (V_s), and presents an open circuit to the ground voltage V_g.

This principle affords the advantage of being able to handle very high voltage differences between signal and amplifer "grounds". Or, when used with bridge and other differential sources, very high common mode voltage levels. A further merit is that its error rejection is independent of any closed loop gain setting, which is certainly not the case for the differential technique to be discussed shortly.

Disadvantages occur through limited bandwidth, which can only be a fraction of the modulation frequency, plus the fact that intermodulation between chopping and signal frequencies can create output errors. Another drawback is that error reducing feedback cannot embrace both modulator and demodulator without restoring the path for ground currents.

The switched capacitor principle, Figure 13B, is an alternative method for breaking the ground loop circuit. This method is analogous to the modulator-demodulator, and tends to provide similar advantages and disadvantages, as well as particularly poor frequency response.

DIFFERENTIAL BALANCING OF GROUND LOOP ERRORS

The most widely-used trick for eliminating ground-loop errors is not so much a process of attenuating ground loop currents, but instead, of applying identical fractions of ground loop voltage to the inverting and noninverting terminals of a differential amplifier. In this way, the ground voltage is applied as a common mode voltage to the differential amplifier, while the transducer signal is applied differentially between the amplifier's input terminals. So long as the amplifier has high common mode rejection, it will ignore the common mode voltage and respond only to the true input signal.

The basic idea and circuit analysis are presented in Figure 14A. Here, the ground

loop currents flow through the parallel paths APB and AQB, adding to the voltages V_1 and V_2 at the amplifier's input terminals. If the signal source is temporarily neglected (removed for example), then V_1 and V_2 will be created solely by the ground loop currents. Accordingly, it will be possible (for DC errors at least), to adjust balance resistor R_B so as to make V_1 exactly equal to V_2. But $V_1 = V_2$ now forms the common mode input voltage for the differential amplifier, which, ideally, develops zero output for identical voltages applied to its inverting and noninverting input terminals. In practice, Figure 14B, the resistors, R, across which the common mode

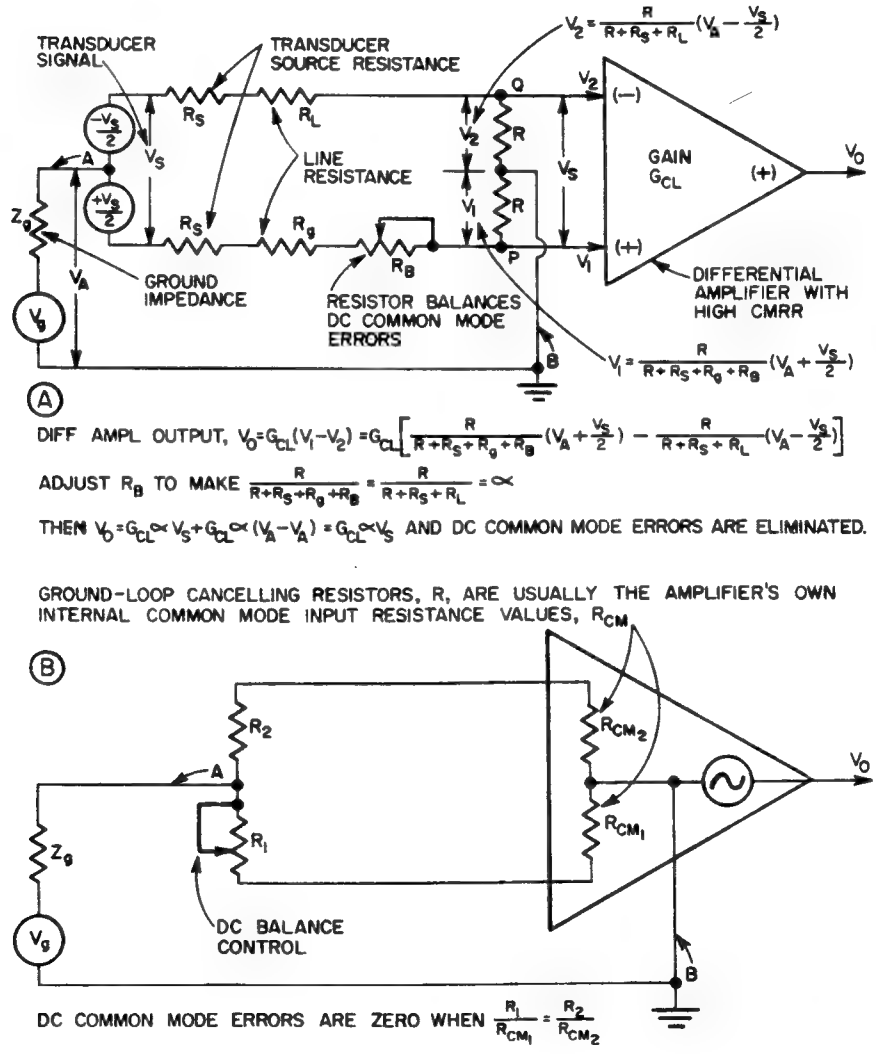


Fig. 14 - Circuit illustrates method for minimizing ground loop errors by converting ground loop voltage into amplifier common mode input voltage. Equal proportions of V_g are applied to inverting and noninverting terminals and their effects scaled down in proportion to amplifier's CMRR (A). In practical circuit, high-value balancing resistors R are replaced by amplifier's own common mode input resistances, Rcm (B). Although method shows only DC balancing, basic principles are also applied in reducing AC ground loop and common mode errors.

voltages V_1 and V_2 are developed are actually the differential amplifier's own common mode input resistances, R_{cm}.

Commercial amplifier's are available with CMRRs of 10^6 or more, thereby reducing every volt of common mode input to a microvolt of equivalent common mode error (shown as e_{cm} in Figure 3C). This performance level makes accuracies of 100 PPM entirely feasible....at least insofar as common mode errors are concerned.

The reader should note that the balancing resistor merely eliminates DC common mode errors, whereas in fact, AC problems are the predominant ones. However, the principles of balancing AC common mode errors are similar, and are discussed more thoroughly in some of the texts listed in the bibliography at the end of this article.

DIFFERENTIAL MEASUREMENT

So far, we have used a differential amplifier as a subtle and economical way to conquer ground loop problems in high accuracy data measurement applications. However, the differential amplifier is also used for data measurements in which the transducer's output is inherently differential rather than single ended.

Strain gauge elements, for example, are usually connected in Wheatstone bridge arrangements, and develop push-pull output signals perched on relatively high levels of common mode voltage. Even when the strain gauge elements are isolated from ground (insofar as leakage capacitance permits), the amplifier must invariably be a differential one in order to extract millivolt signals from several volts of common mode "carrier". Biomedical applications too, invariably require differential amplifiers in order to extract information from high levels of 60Hz pickup.

CM ERROR CAUSED BY SOURCE UNBALANCE

Three sources of common mode error were discussed in the section on differential amplifiers, and the common mode errors for various differential configurations were listed in Table 1. There is, however, a fourth common mode error that can arise even when an infinite CMRR amplifier is put to work in a practical data gathering application. The error stems from unequal amounts of source impedance in series with the amplifier's input terminals.

For example, if the signal transducer is operated with one of its output terminals grounded (point A in Figure 15), then its internal resistance or impedance is placed is placed in series with the amplifier's inverting terminal. Even though the two signal lines introduce further series resistance, resistance imbalance will remain if the source resistance is appreciably higher than the signal line resistances. The net imbalance is represented as R_u in Figure 15.

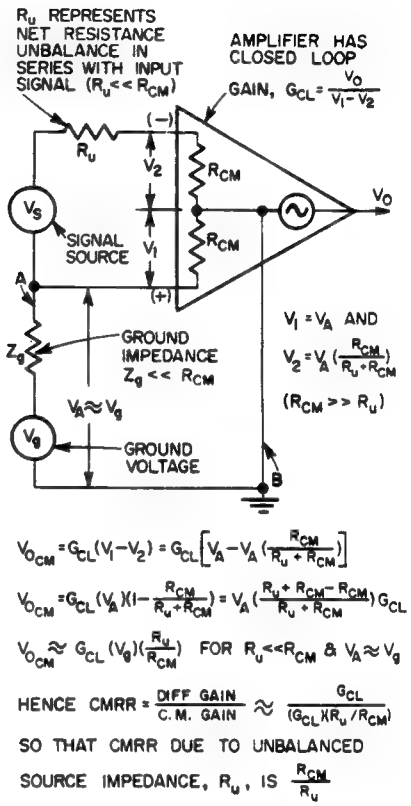


Fig. 15 - Differential method can reject common mode errors when working with single-ended sources, although resistance imbalance impairs rejection process. Overall CMRR is maximized by making amplifier's common mode input resistance very high compared with resistance unbalance.

Theoretically, of course, it would be possible to introduce a compensating resistance into the noninverting line to cancel the effect of R_u, just as in Figure 14. But in practice this is not always so simple. What happens, for example, when the amplifier is switched sequentially to read the output from an array of different transducers, all with different amounts of imbalance? Or what happens when signals are developed by an inductive-type transducer (e.g., tape recorder head), whose internal impedance varies with ground-loop and common mode frequency. In both these instances, and in many more, common mode and ground loop errors cannot be completely compensated.

Actually, the degree of common mode error does not depend upon the absolute value of resistance unbalance. As the analysis of Figure 15 shows, the error is proportional to the ratio of source resistance imbalance R_u to amplifier input resistance R_{cm}, R_u/R_{cm}. Consequently, the higher the amplifier's common mode input resistance, R_{cm}, the smaller will the common mode errors become. The solution, therefore, in absence of methods for external common mode compensation, is to make the amplifier's common mode input resistance as high as possible.

Typical amplifiers are rated for common mode errors with a given amount of source resistance unbalance. Often, this value for R_u is 1000 ohms. In order to provide 10^6 CMRR with such a value of imbalance requires a minimum common mode input resistance of R_{cm} = CMRR x R_u = 10^9 ohms.

If such an amplifier is used to measure 10 millivolt signals against a 5 volt common mode background, then the equivalent common mode input error, e_{cm}, becomes

$$5\ V/10^6 = 5\ uV.$$

The percentage measuring error, 100% x e_{cm}/V_s works out to

$$100\% \times 5 \times 10^{-6}/10^{-2} = 0.05\%$$

SOURCE LOADING ERROR

The amplifier's finite differential input resistance (usually smaller than the common mode input resistance), creates an attenuating effect when measuring signals from sources having appreciable internal resistance or impedance. In turn, this attenuating effect leads to a measuring error, termed source-loading error, equal to R_S/R_{IN} where these symbols represent source resistance and amplifier differential input resistance.

Using the same amplifier referred to above, and assuming a 1000 ohm total source resistance (not just source unbalance), then the differential input resistance R_{IN} must be higher than 10^6 ohms if the loading error is to be held below 0.1%. (Percentage loading error = 100% x R_S/R_{IN}.)

So not only must the amplifier's common mode input resistance be very high to reduce

common mode errors caused by source unbalance, but the differential input resistance must also be very high to minimize source loading errors.

RESPONSE, GAIN & DRIFT

Although most data amplifiers are used for narrow bandwidth measurements from DC to perhaps 500Hz, the response characteristics enter the picture when the amplifier is used to sample readings from several signal sources. Recovery, slewing and settling times then define the maximum rate at which the amplifier can be commutated between the various sources.

Adjustable gain enables the user to scale the amplifier's output signal to represent convenient units of the phenomenon he is measuring. Thus, each volt of amplifier output might represent 1 ton of thrust, 1°C of temperature rise, 32.2 Ft/Sec of velocity, or any other natural variable. Since accuracy depends upon the gain linearity, a considerable amount of negative feedback must be used to achieve the desired linearity levels.

Drift is a major parameter in determining the measurement accuracy. If an amplifier with 2uV/°C maximum drift operates over the temperature range 25°C to 35°C, the equivalent input error is 10 x 2 = 20uV, which creates a further

$$100\% \times 20 \times 10^{-6}/10^{-2} = 0.2 \text{ Percent}$$

measuring error for 10mV signals.

Current drift, or "pump out" current must also be considered when the source impedance is appreciable. For example, if the total source impedance is 10,000 ohms, then the input error caused by 300 pA/°C current drift for a $\pm$10°C range is

$$10{,}000 \times 300 \times 10^{-12} \times 10 = 30 \text{ uV}$$

This will create a $100\% \times 30 \times 10^{-6}/100 \times 10^{-3} = 0.03\%$ measuring error.

Actually, a source impedance of 10^4 ohms could create serious loading errors, and if single ended, substantial common mode errors too.

CONCLUSION

We have established that a circuit cable of measuring millivolt signals in the presence of several volts of common mode or ground loop noise must have low drift, high CMRR, high input impedance, fast response, and variable gain. The next step is to see how conventional operational amplifier circuits fulfill these basic requirements.

IMPEDANCE

The need for impedance levels of 1000 megohms or more rules out a differential amplifier based on the inverting circuit Figure 8B whose input impedance is equal to the circuit's input resistance, R_1, Figure 1.

A noninverting circuit, Figure 2 can provide adequate input impedance when used in either of the differential amplifiers, Figure 8A, or Figure 10, so the next parameters to consider are DC stability, response, gain, and most important, CMRR.

DRIFT

The question of DC stability rests upon the drift of the two operational amplifiers selected for the differential circuit used. Chopper stabilized op amps introduce complications because of their single endedness: they require special power supplies to overcome this limitation. Alternatively, high stability but conventional differential op amps might be used. It is conceivable that a pair of ordinary op amps could provide adequate input DC stability and as a matter of fact, input impedance too. For example, Analog's Model 180B features 0.75 uV/^{o}C drift and 1000 megohms Z_{cm}, while FET type 147C gives 2 uV/^{o}C drift and better than 10^{11} common mode input impedance.

RESPONSE

Many operational amplifiers can provide good response, in combination with the prerequisite DC stability and input impedance. Analog's Model 180B is such a unit, as is the FET amplifier Model 147C. Thus, response is no particular stumbling block for

the use of op amps as building blocks in advanced data acquisition circuits.

SCALING FACTOR (GAIN)

The amount of closed loop gain and gain linearity that an amplifier can provide, depends upon the amount of open loop gain available for use as gain-stabilizing negative feedback.

The relationship between closed loop gain stability, $\% \triangle G_{cl}/G_{cl}$, and open loop gain variation, $\% \triangle A/A$, is

$$\% \triangle G_{cl}/G_{cl} = \% \triangle A/A \times 1/(1 + A\beta)$$

where β is the fraction of open loop gain used as feedback.

Because $1/\beta$ is very nearly the same thing as closed loop gain G_{cl}, and $A\beta \gg 1$, the above equation simplifies to

$$\% \triangle G_{cl}/G_{cl} \approx \% \triangle A/A \times G_{cl}/A.$$

If the data amplifier must provide 2000 volts/volt gain for DC signal scaling, and specifications call for 0.05% gain linearity, the stability equation can be manipulated to give the nominal value of open loop DC gain A in terms of the amplifier's expected open loop gain variation, $\% \triangle A/A$.

For example, if open loop gain varies by 25% due to loading, aging or temperature effects, that is $100\% \triangle A/A = 25\%$, then $0.05\% \approx 25\% \times 2000/A$. This equation shows that the minimum open loop gain A under these conditions: $25 \times 2000 \div 0.05 = 10^6$, or 120 dB, begins to get beyond the range of the types capable of giving adequate stability.

Note: The chopper stabilized amplifier is an exception. Most chopper stabilized types feature very high DC gain along with advanced drift specifications. Chopper types also provide very fast response. Unfortunately, however, the chopper stabilized op amp requires elaborate power supply arrangements when used in high impedance differential circuitry.

Consequently, unless the stability specifications are relaxed to enable a high gain amplifier to be used (e.g., Model 102 at 5 uV/°C max drift and 10^6 gain), high values of closed loop gain will tend to put a two amplifier differential circuit (Figure 8A) beyond the reach of most off-the-shelf op amps.

On the other hand, if the total 2000 gain is shared between two separate amplification stages, as occurs in the differential circuit of Figure 10, then Models 180B or 147C are back in the running once more. Cost for three such amplifiers, however, would begin to nudge $350, which gets a bit uneconomical.

COMMON MODE REJECTION

This is the specification that really inhibits the use of conventional op amps in differential data measuring circuits. Unfortunately, there are very few operational amplifiers with CMRR beyond about 500,000 : 1 (Analog's varactor bridge Model 301, with 10^8 CMRR at DC, is an exception), while those op amps emphasizing CMRR tend to suffer from high cost, or deficiencies in some other parameter. (Model 301 costs $198 and features 50 uV/°C drift: it handles ultra-high source impedances when connected in either Figure 8A or Figure 10.)

However, for more practical applications, where the signal source is a low impedance thermocouple of strain gauge bridge, no presently available operational amplifier model fits the CMRR requirements and at the same time features high stability, open loop gain, input impedance, fast response, all at moderate cost.

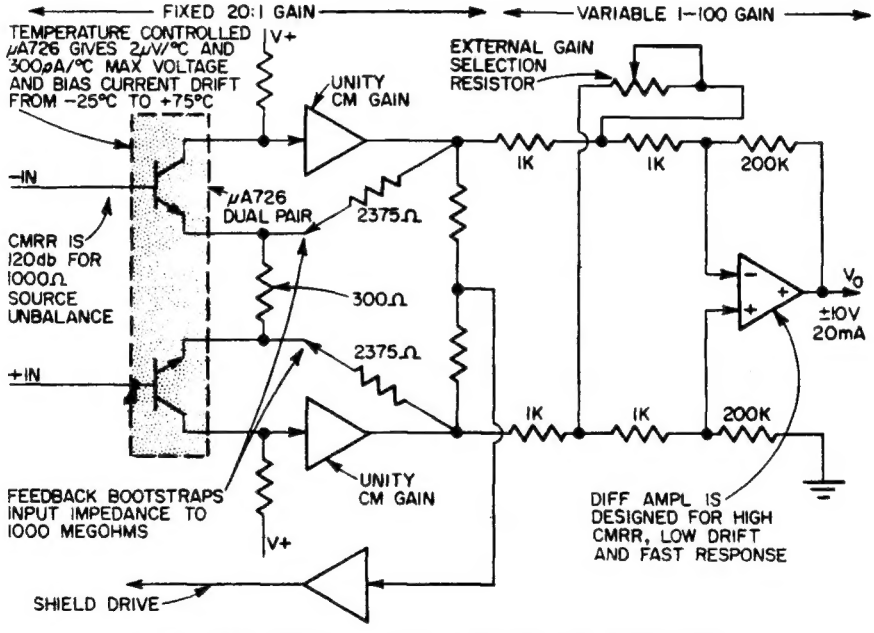
In summary, therefore, a data amplifier must be designed from the ground up, in order to achieve adequate performance at reasonable cost. Operational amplifiers used as data amplifier building blocks cannot meet cost and performance specs if such features as 10^6 CMRR, 2000 maximum gain, 10^9 and 10^7 common mode and differential input impedance, and 2 uV/°C drift are required.

NEW DATA AMPLIFIER MODEL 601

Analog Devices has applied its knowhow in designing high density semiconductor circuits to the data amplifier problem. Using temperature compensated uA726 dual tran-

sistor pair as the input stage, an advanced data amplifier Model 601 has been developed, and features the specifications outlined in the foregoing paragraph. Its basic circuit, Figure 16, follows the general principles of the two stage differential design outlined in Figure 10. (An alternative version, Model 602, with slightly relaxed drift and gain specs, is also available, and based on the noninverting circuit of Figure 8A.)

Both these amplifiers are fully encapsulated into PC mounting modules that operate from -25°C to +75°C, and which can be located right at the signal source. They also save an enormous amount of mechanical hardware (racks, supports, interconnecting sockets and cables), by mounting direcly into the data handling equipment.



MODEL 601 WIDEBAND DIFFERENTIAL DC AMPLIFIER

Fig. 16 - Wideband differential DC amplifier Model 601 embodies many of the principles outlined in this article. Input circuit based on uA726 temperature compensated monolithic pair provides high voltage & current stability, uses bootstrapping feedback to create 1000 megohms common mode and 10 megohms differential input impedance. Subsequent circuitry preserves uA726's inherently-wide bandwidth by using low-value resistors, which also permit highest resistance stability, hence best long-term CMRR. Single resistor adjusts closed-loop gain from 20 to 2000; fixed first-stage gain of 20:1 reduces second stage's gain-inequality error: $CMRR_A = A/(A_2 - A_1)$, twentyfold.

BIBLIOGRAPHY

Advantages of Direct-Coupled Differential Data Amplifiers, Morton H. Levin; Hewlett-Packard Journal, July 1967. 3 pages.

Application Notes for Differential DC Amplifiers; Dynamics Instrumentation Company, 583 Monterey Pass Road, Monterey Park, California. 3 pages.

Common Mode Rejection, Peter Pohl; Dynamic Instrumentation, 801 So. Arroyo Parkway, Pasadena, California. 1963. 5 pages.

Designing for Low Level Inputs, D.B. Schneider, Neff Instrument Corp., 1088 East Hamilton Rd., Duarte, California. Reprinted from ELECTRONIC INDUSTRIES, January 1961. 5 pages.

Differential Amplification, Applications ZA-102; Zeltex, Inc., 1000 Chalomar Road, Concord, California. 11 pages.

EID Surveys the Scope of Instrumentation Amplifiers, Ralph Morrison, Dynamics Instrumentation Company. Reprinted from Electronic Instrument Digest, March 1967. 8 pages.

Errors in Data Amplifier Systems, Richard Y. Moss II; Hewlett-Packard Journal, July 1967. 4 pages.

Floating Power Supplies, Applications ZA-103; Zeltex, Inc., 1000 Chalomar Road, Concord, California. 6 Pages.

Ground Loops (Electrical): The General Case and an Example, E. L. Stewart; Analog Report No. 15, July 1963. 11 pages.

Grounding Low-Level Instrumentation Systems---A Coherent Philosophy, the EID Staff with the assistance of Mr. D. H. Sheingold, Consulting Editor, Amplifiers & Transducers; Electronic Instrument Digest, January-February 1966. 4 pates.

Instrumentation Amplifiers: A Survey, Staff Report; Electromechanical Design, March 1967. 5 pages.

Isolating the Causes of Common-Mode Noise, R. B. Fradella, Giannini Controls Corp., Duarte, Calif.; Electronic Design, August 1963. 4 pages.

The Measurement of Small Signals in the Presence of Common Mode Interference, L. V. Mayhead, Digital Measurements Ltd; Electronic Engineering, July 1962. 3 pages.

Minimizing Common-Mode Noise; Control Engineering Data File 117, July 1967. 2 pages.

Noise Control in Low Level Data Systems, A.S. Buchman, Radio Corporation of America; Electromechanical Design, September 1962. 18 pages.

Selecting a Differential Amplifier, Ralph Morrison, Dynamics Instrumentation Company, 583 Monterey Pass Road, Monterey Park, California. 4 pages.

Shielding and Grounding for Instrumentation Systems, Ralph Morrison, Dynamics Instrumentation Co., 583 Monterey Pass Road, Monterey Park, California. 8 pages.

Source and Load Impedance: Effects on Closed-Loop Characteristics, Ronald R. Jennings, U.S. Naval Avionics Facility; Reprinted from ET Electro-Technology, September 1966. 7 pages.

Straight Talk About Data Amplifiers, Jim Rose; EDN Magazine, November 23, 1966. 8 pages.

DESCRIPTION

The Model 601 is a modular encapsulated low level differential amplifier specifically designed for data acquisition applications or for instrumentation applications which require high input impedance, differential inputs and high common mode rejection. This module differs from operational amplifiers in as much as internal feedback networks are included to give a closed loop gain from 20 to 2000. Gain is changed by varying a single external resistor. In many applications the small modular package, 3.5 x 2.5 x 0.875 in., can be located near the transducer or source voltage to reduce noise pick-up problems.

The Model 602 is a lower cost version in a smaller encapsulated package. It is primarily intended for less demanding applications and offers substantial cost savings with some compromise in specifications and application flexibility. The 602 offers fixed gains of 10 or 100, common mode rejection of 100dB and 10V output. The most significant features are its small size (1.5 x 1.5 x 0.62 in.) and low cost.

SPECIFICATIONS (typical @ ±15VDC and 25°C and gain of 2000(601) , 100(602-100) and 10(602-10) unless noted)

	601	602-A/B-100	602-A-10
GAIN CHARACTERISTICS			
Range	20-2000 (selected by external resistor)	100-1000 (selected by external resistor)	10-100 (selected by external resistor)
Accuracy	adj. to ±.01% by external gain pot	Internally trimmed to 0.05% max @ gain-of-100	Internally trimmed to ±0.05% max @ gain-of-10
Stability	±.02%/month	±.02%/month	±.02%/month
Temperature Coefficient	±.003%/°C	±.001%/°C	±.001%/°C
Nonlinearity @ DC	±.02% (best straight line)	±.01% (best straight line)	±.01% (best straight line)
OFFSET CHARACTERISTICS			
Offset Voltage			
Initial Offset, 25°C, max	±150μV RTI (adj. to 0)[1]	±200μV/±100μV RTI (adj. to 0)[1]	±300μV RTI (adj. to 0)[1]
Temperature Drift, max	2μV/°C RTI plus 2mV/°C RTO	±10μV/°C/±2μV/°C RTI	±10μV/°C RTI
Drift Stability - per day	±10mV RTO	±10μV RTI	±10μV RTI
Supply, Voltage Influence	±20μV/% RTI (3k source)	±10μV/% RTI (1k source)	±10μV/% RTI (1k source)
Bias Current (each input)			
Initial, 25°C,max	±10nA	±50nA	±50nA
Temperature Drift, max[2]	±300pA/°C	±1nA/°C	±1nA/°C
INPUT CHARACTERISTICS			
Full Scale Voltage Range	±(5-100)mV	±(10-100)mV	±(100-1000)mV
Differential Impedance	10MΩ paralleled with 1000pF	1000MΩ paralleled with 50pF	1000MΩ paralleled with 50pF
Overvoltage, max	±10V (with no damage)	±20V differential,±20V each input to ground	±20V differential, ±20V each input to ground
CMRR, min @ ±10V	120dB, DC-60Hz (1k source unbalance)	100dB, DC-60Hz (1k source unbalance) 86dB,DC-500Hz(1k source unbalance)	80dB,DC-60Hz(1k source unbalance) 75dB,DC-500Hz(1k source unbalance)
OUTPUT CHARACTERISTICS			
Output Rating	±10V @ 20mA(DC to 20kHz)	±10V @ 4mA (DC to 10kHz)min	±10V @ 4mA (DC to 8kHz) min
Output Resistance	0.5 ohms	0.5 ohms	0.5 ohms
Short Circuit Limit	±100mA	±70mA	±70mA
RESPONSE CHARACTERISTICS			
Frequency Response	1% from DC-1kHz ±3dB from DC-30kHz } all gains	-1% from DC-250Hz(gain-of-1000) -1% from DC-1kHz(gain-of-100) -3dB from DC-75kHz(gain-of-100) -3dB from DC-20kHz(gain-of-1000)	-1% from DC-500Hz(gain-of-100) -1% from DC-1kHz(gain-of-10) -3dB from DC-75kHz(gain-of-10) -3dB from DC-35kHz(gain-of-100)
Settling Time to 0.1%	100μsec for full scale step	50μsec	50μsec
Overload Recovery	1msec	200μsec	200μsec
POWER REQUIREMENTS			
Supply Voltage	±(15 to 16)VDC	±(15 to 16)VDC	±(15 to 16)VDC
Supply Current,max	60mA Quiescent	14mA Quiescent	14mA Quiescent
PRICE			
(1-9)	Contact factory	Contact factory	Contact factory
(10-24)			

1. With external pot.

2. Avg. from -25°C to +75°C(601); avg. from 0°C to 70°C(602)

Note: Specifications subject to change without notice.